PL2303GR
Single-chip USB to RS-485 IC with GPIO

USB Interface

- Fully Compliant with USB 2.0 specification (Full-Speed Mode).
- UHCI/OHCI (USB 1.1), EHCI (USB 2.0), xHCI (USB 3.1) Host Controller Compatible.
- Provides royalty-free USB to Virtual Com Port (VCP) drivers for Windows, Mac, Linux, and Android.
- Highly integrated USB 1.1 FS Transceiver. Integrated termination resistors and pull-up resistor to reduce PCB external components.
- Supports 256-byte OTPROM (One-Time Programmable ROM) for USB device descriptors and GPIO custom configuration. OTPROM can be programmed directly through USB port.
- Each IC has unique ID (for Serial Number).
- Supports bus-power, self-power and high-power USB device configuration.
- Supports Windows USB Selective Suspend (Remote Wakeup enabled).
- HBM ±8kV ESD Protection for all pins.
- MM ±400V ESD Protection for all pins.
- Supports Windows USB Selective Suspend (Remote Wakeup enabled).
- Supports Windows Modern Standby.
- Bind a specific COM port number (1~65,535) and product string via OTPROM / EEPROM (no need to submit WHQL certification and pay additional fees).
- Expand COM port number range: from 1~255 to 1~65,535.
- “Product String” of OTP tool support multiple language.

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-I/O functions.
- Configurable I/O pin output driving strength.
- Total 4 General Purpose I/O (GPIO) pins can be used after configured.
- Optional Clock Output to external MCU.
- Supports 5V tolerance which allows 5V input signal.

RS-485 Interface

- Support one pair differential RS-485 Interface:
  - Half Duplex
  - Flexible baud rate from 1 bps to 10M bps
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and a half, or two stop bits
  - Software Flow Control (XON/XOFF)
- 1024-byte bi-directional data FIFO buffers (768-byte receive/256-byte transmit) for faster data throughput. Configurable in OTPROM.
- Configurable Transmit and Receive LED pins.
- Integrated Transient Voltage Suppressor (TVS) in the RS-485 transceiver and ESD Protection Voltage for RS-485 bus pins
  ±15 kV, IEC 61000-4-2, Criteria B, Contact Discharge
  ±18 kV, IEC 61000-4-2, Criteria B, Air-Gap Discharge
  ±15 kV, EIA/JEDEC, Human Body Model

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Document Version 1.0.1

Miscellaneous

- Integrated self-generated precise clock generator. External crystal is optional.
- Integrated Power-on-Reset (POR) circuit.
- Integrated 5V to 3.3V LDO that can support 80mA for external components.
- Low operating power and USB suspend current.
- -40ºC to 85ºC Operating Temperature.
- 28-pin SSOP package (RoHS compliant and Pb-free Green Compound).

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REVISION HISTORY

Revision	Description	Date
1.0.1	➢ Added support for COM port numbers up to 65,535. ➢ Added the ability for manufacturers to customize product strings in multiple languages (without needing to reapply for WHQL certification or pay additional fees).	2025/12/24
1.0.0	➢ Formal release	2021/3/15

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Product Data Sheet **PL2303GR**

1. Product Applications

- USB to RS-485 converters/cables/dongles/adapters
- Industrial PC, system and device
- Automation Networks

2. Royalty-Free Driver Support

- Windows 10, 8, 7(Microsoft Certified WHQL Drivers)
  - Windows Update Driver installation available in Windows 7 and above (32/64-bit)
- Windows Sever 2008 R2, 2012, 2016, 2019
- Windows Embedded Industry, Point-of-Service (WEPOS), and POSReady
- Windows Embedded Compact, Windows Embedded CE, Windows CE
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2303GR	28-pin SSOP	PL2303G4ZJG7P7	48pcs / tube
		PL2303G4ZJG8P7	2000pcs / reel

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4. Block Diagram

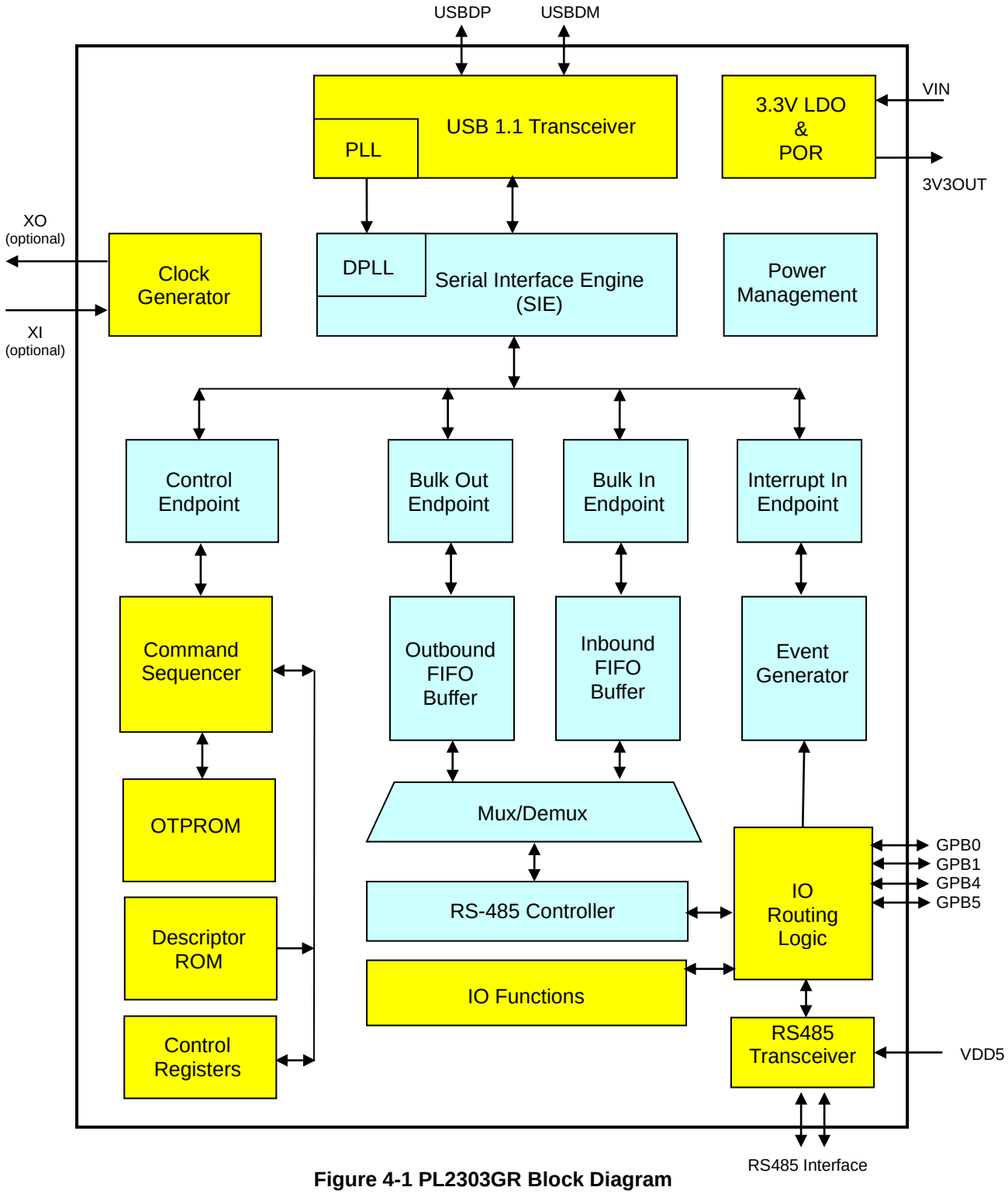

Figure 4-1 PL2303GR Block Diagram

5. USB Logo Certification

(TBA)

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6. Overview

The new PL2303GR chip is one of the latest G-Series IC product added to the popular PL2303 USB to Serial Bridge Controller family. It provides an advanced full-featured single-chip bridge solution for connecting a Half-Duplex RS-485 interface device to any Universal Serial Bus (USB) capable host. The PL2303GR provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most operating systems so that the application software can communicate with the USB to RS485 device via the virtual COM port.

It also integrates an internal precise clock generator (no external crystal required), USB 1.1 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and OTPROM.

The PL2303GR added several new features and enhancements:

- Integrated termination resistors and pull-up resistor to reduce PCB external components.
- New USB drivers for different OS platforms with faster performance and advanced features.
- Precise baud rate generator (up to 10Mbps).
- OTPROM can be programmed directly through USB (no high voltage generator required).
- Larger TX/RX FIFO data buffers (1024-byte).
- Up to 4 configurable GPIO pins.
- Versatile GPIO functions and routing logic (TX/RX LED, CLK_OUT, etc.).
- Configurable output driving strength of GPIO pins.
- Each IC has unique ID (for Serial Number).

The PL2303GR is designed to provide one pair of Half-Duplex differential RS-485 interface. It provides a small footprint that could easily fit in to any connectors and handheld devices. With very small power consumption in either operating or suspend mode, the PL2303GR is perfect for bus powered operation with plenty of power left for the attached devices.

The PL2303GR has a half-duplex RS-485 transceiver with the ESD protection of ±15kV (IEC 61000-4-2, contact discharge). This RS-485 transceiver is fully compliant with the EIA/TIA-485 standard with 5V power supply. The RS-485 transceiver features a fail-safe receiver, which guarantees the output of the receiver to be logic high when the differential inputs (A and B) of the receiver are open, short or idle under abnormal operating conditions.

The RS-485 transceiver features a hot-swap glitch-free design which guarantees outputs of the transmitter and the receiver in a high impedance state and even no short current event during the power up period. It has the thermal shutdown and the current limited function in the transmitter to protect the device from damage by system fault conditions during normal operating condition. It is designed 1/8 unit load with minimum 96kohm of input impedance, which can connect 256 devices on a bus.

The PL2303GR is available for Pb-free (RoHS compliant) green compound package of 28-pin SSOP.

6.1 PL2303 G-Series USB to Serial Family Product Table

Prolific's new PL2303 G-series USB to Serial family product line offers a variety of new advanced features for USB serial interface product design. The PL2303 G-series are redesigned to provide accurate and flexible baud rate support as well as plenty of I/O functions that can be easily configured in OTPROM memory.

PL2303 G-Series USB to Serial Family Product Line						
Product	**PL2303GC**	**PL2303GS**	**PL2303GE**	**PL2303GT**	**PL2303GL**	**PL2303GR**
Description	USB to Full UART (Integrated Clock)	USB to Full UART (Integrated Clock)	USB to Full UART (High ESD Protection)	USB to RS232 (Internal RS232 Transceiver)	USB to Basic UART (Low-Pin Count)	**USB to RS-485 (Internal RS-485 Transceiver)**
Packages	SSOP28 UQFN24	SSOP16	SSOP28	SSOP28	SOP8	**SSOP28**
UART Interface	RS232 RS422/RS-485	RS232 RS422/RS-485	RS232 RS422/RS-485	RS232 Only	RS232 (TX-RX Only)	**RS-485 Only**
Max. Data Rates	12Mbps	12Mbps	12Mbps	1Mbps	115200bps	**10Mbps**
Dedicated GPIO Pins	6	0	6	4	0	**4**
Shared GPIO (with UART pins)	9	9	9	0	0	**0**
Clocking	Internal[1]	Internal	Internal[1]	Internal	Internal	**Internal**
OTPROM[2]	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data	**USB Data**
External EEPROM Option	YES[3]	YES[3]	YES[3]	YES[3]	NO	**NO**
Android OS Support	YES	YES	YES	YES	YES	**YES**
Configurable Data Buffer[4]	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	**768-byte (RX) 256-byte (TX)**
Battery Charger Detection Option	YES	YES	YES	No	No	**No**
I/O Voltage Range	I/O levels from 1.8V to 5V	I/O levels from 1.8V to 5V	I/O levels from 1.8V to 5V	3.3V	I/O levels from 1.8V to 5V	**3.3V**
Pin Compatible	PL2303HXD (SSOP28 only)	New design	PL2303EA	PL2303RA	PL2303SA	**New design**

[1] – Also supports external crystal clock source to bypass internal clock.

[2] – OTPROM allows setting the USB data descriptors. Also allows setting of multi-function GPIO options.

[3] – External EEPROM (when enabled in OTPROM) will override OTPROM settings.

[4] – TX/RX data buffers are configurable in OTPROM (PL2303GC, PL2303GS, and PL2303GE, PL2303GR); or by driver customization.

7. Pin Diagram and Description

7.1 SSOP28 Pin Diagram

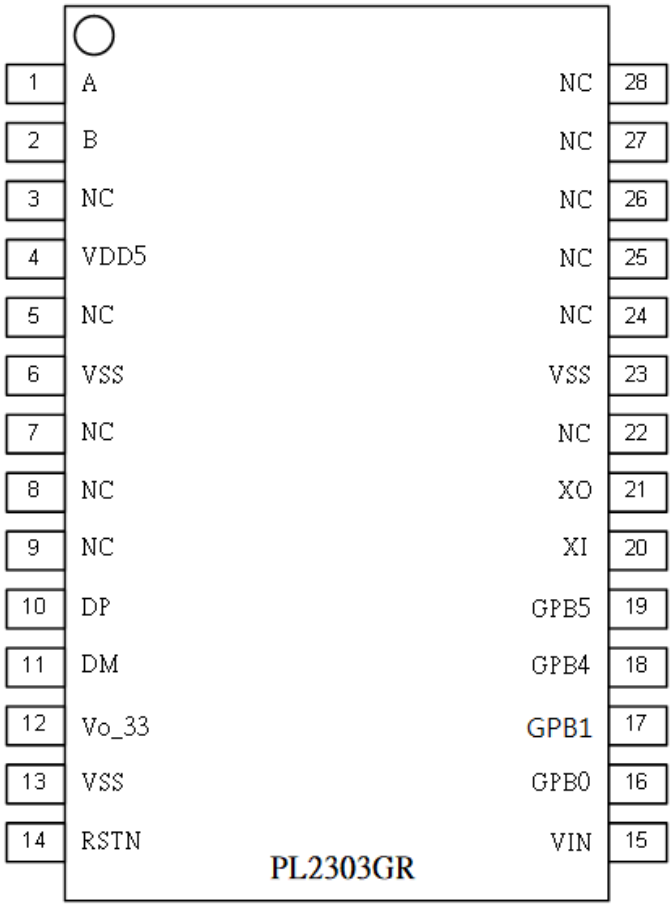


Figure 7-1 PL2303GR Pin Diagram (SSOP28)

7.2 Pin-Out Description

Table 7-1: USB Data Interface Pins

Pin Name	Pin No.	Type	Description
DP	10	I/O	USB Port Data Plus (D+) Signal.
DM	11	I/O	USB Port Data Minus (D-) Signal.

Table 7-2: RS-485 (Serial Port) Interface Pins

Pin Name	Pin No.	Type	Description
A	1	I/O	Non-inverting Receiver Input and Non-inverting Transmitter Output
B	2	I/O	Inverting Receiver Input and Inverting Transmitter Output

Table 7-3: Configurable GPIO Pins – Group B

Pin Name	Pin No.	Type	Description
GPB0	16	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB1	17	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB4	18	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB5	19	I/O	Configurable GPIO Pin. (see Section 7.4)

NOTE: All GPB pins are default Input mode (except GPB6).

Table 7-4: Power and Ground Pins

Pin Name	Pin No.	Type	Description
VDD5	4	Power	RS-485 power supply input.
VO_33	12	Power	+3.3V output power from integrated LDO regulator.
GND	6, 13, 23	Power	Ground
VIN	15	Power	USB port VBUS power supply input.

Table 7-5: Miscellaneous Pins

Pin Name	Pin No.	Type	Description
RESET_N	19	Input	Active low Reset pin. Can be used by external device to reset the PL2303GR. NOTE: This pin has internal pull-high. It can be pull up to VIN or VO_33.
XI	27	Input	Optional. 12MHz crystal oscillator input. If not used, leave pin floating.
XO	28	Output	Optional. 12MHz crystal oscillator output If not used, leave pin floating.
NC	3, 5, 7~9, 22, 24~28	NC	No internal connection. Leave floating.

7.3 GPIO Multi-Function Options

The PL2303GR chip (SSOP28 package) provides a total of 4 configurable GPIO (General Purpose I/O) pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the OTPROM of the PL2303GR. When these pins are configured as standard GPIO pins, customers can refer to the Prolific GPIO SDK (software development kit) to develop software to control the GPIO pins for customer application desired functions.

Table 7-6: Configurable GPIO Multi-Function Pins

GPIO	Pin No.	Factory Default	Configurable Options (using OTPROM Tool)				
GPB0	16	GPIO Input Pin	TX_LED	CLK_OUT			
GPB1	17	GPIO Input Pin	RX_LED	TRX_LED			
GPB4	18	GPIO Input Pin	CLK_OUT				
GPB5	19	GPIO Input Pin					

Table 7-7: GPIO Multi-Function Option Descriptions

GPIO Function	GPIO Pins	Type	Description
TX_LED	GPB0 (Pin 16)	Output	Serial Port: TXD Access LED.
RX_LED	GPB1 (Pin 17)	Output	Serial Port: RXD Access LED.
TRX_LED	GPB1 (Pin 17)	Output	Serial Port: TXD and RXD Access LED.
CLK_OUT	GPB0 (Pin 16) GPB4 (Pin 18)	Output	This pin can generate clock output up to 12MHz. Clock rates can be configured in OTPROM or customized driver. **Note: Only one GPIO pin can be configured as CLK_OUT function.**

8. Functional Description

This section details the functional block diagram description of the PL2303GR.

8.1 USB 1.1 FS Transceiver

The USB Transceiver provides the USB full-speed electrical signal requirements and USB physical interface (DP/DM). This block also includes one precise internal oscillator for PLL. The PLL provides the clock to other logic functions. This block also includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal.

8.2 LDO Regulator

This block is the 5V to 3.3V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components.

8.3 Clock Generator

The clock generator module generates the 48MHz and 12MHz reference clock signals for internal chip logic. The internal clocks will be stopped while in suspend state.

8.4 USB FS SIE

The USB Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB FS transceiver to parallel data for internal circuit. This block supports USB packet decoding and encoding. It also generates and check packet CRC, bit stuffing, SYNC and EOP frame signal. The DPLL module will use the internal 48MHz clock to synchronize external DP/DM transitions to generate 12MHz clock for USB interface related circuit.

8.5 Power Management

This module will monitor the USB attachment and DP/DM signals state to create reset state, running state, suspend state, wakeup state, etc.

8.6 Control Endpoint

The Control Endpoint module handles control endpoint packet transfer protocols such as SETUP packet, DATA packet and return status packet.

8.7 Bulk Out Endpoint

The Bulk Out Endpoint module handles bulk-out endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers USB host bulk-out data to chip outbound FIFO.

8.8 Bulk In Endpoint

The Bulk In Endpoint module handles bulk-in endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers data inside the chip inbound FIFO to USB host through bulk-in DATA packet.

8.9 Interrupt In Endpoint

The Interrupt In Endpoint module handles interrupt-in endpoint packet transfer protocols such as DATA packet and return status packet. It transfers interrupt data generated inside the chip to USB host through interrupt-in DATA packet.

8.10 Command Sequencer

This module handles the USB standard requests and vendor requests. It dispatches control signals to relative peripheral modules and gather information from peripheral modules. When it received USB standard request commands, it may check ROM data or data latched from OTP and return them to USB host. When vendor requests are received, it dispatches to peripherals to set or get something.

8.11 Outbound FIFO

This buffer receives data from Bulk Out Endpoint and provides data to peripheral modules. It handles read and write pointers and calculate full and empty conditions. There are also near empty threshold check to notify peripheral module that FIFO is going to empty.

8.12 Inbound FIFO

This buffer receives data from peripheral modules and provides data to Bulk In Endpoint. It handles read and write pointers and calculate full and empty conditions. There are also near full threshold check to notify peripheral module that FIFO is going to full.

8.13 Event Generator

This module provides interrupt data to Interrupt In Endpoint. This module senses interrupt event toggle from UART peripheral and GPIO module.

8.14 Internal OTPROM

The OTPROM (One-Time Programming Read-Only Memory) is used to store chip function settings, GPIO pin function setting and USB descriptor related data. A one-time programming user area of the memory is available to allow customization of settings. The user area of the PL2303GR OTPROM can now be easily programmed using the Prolific OTPROM software through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM configuration settings.

8.15 Mux/Demux

This module is designed to pass data between FIFO and RS-485 controller.

8.16 Descriptor ROM

This block contains the USB descriptor data for returning to USB host.

8.17 RS-485 Control

The RS-485 Control module handles the data transfer according to RS-485 format and interface. This module includes a precise baud rate generator that can generate baud rates up to 10Mbps. The baud rate is set from USB command.

8.18 Control Registers

The Control Registers module contains the chip control registers read and set, and initially loads from OTPROM. USB host will use USB vendor command to read and write control registers to set chip function.

8.19 IO Functions

The IO Functions block implements generic GPIO function and many configurable I/O functions such as TX access LED and RX access LED features, clock output features, and others (see Section 7.4).

8.20 I/O Routing Logic

The PL2303GR has many versatile I/O functions. Each GPIO pin is provided with multiple functions that can be configured in the OTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

8.21 RS-485 Transceiver

The PL2303GR is integrated with a half-duplex RS-485 transceiver with IEC61000-4-2 contact ±15kV ESD protection for pins A and B, which contains one transmitter and one receiver inside with 5V power supply. This device is fully compliant with the EIA/TIA-485 standard. The PL2303GR features the hot-swap glitch free design which guarantees the outputs of the transceiver in a high impedance state during the power-up period until the supply voltage has stabilized.

Transmitter

The design of the transmitter is a non-inverted translator that converts the single-ended TTL input signal to differential EIA/TIA-485 signal level. The transmitter of the PL2303GR guarantees up to 10Mbps data rate communication. The differential output voltage VA-VB (VOD2) of the PL2303GR is 2.3V with 54 ohm load under VDD5 = 5.0V, T= 25°C.

Receiver

The receiver of the PL2303GR converts the differential EIA/TIA-485 signals to single-end output TTL signal when receiver is in active state, which incorporates input filtering in addition to input hysteresis. The input filtering enhances the noise immunity under normal operating condition.

True Fail-Safe

In traditional design, the fail-safe function is implemented by two resistors on the PCB. One resistor is terminated pin A to VCC; the other is terminated pin B to GND to keep the receiver output at high state when bus is idle, which is only the open fail-safe.

The PL2303GR guarantees the receiver output high when the receiver inputs are short, open or idle, that is true fail-safe. The threshold voltage of receiver input is between -50mV and -200mV. If the differential input voltage (A - B) of receiver is greater than or equal to -50mV, the receiver output is logic-high. If (A - B) is less than or equal to -200mV, the receiver output is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage (A - B) is 0V, so the receiver output is logic-high at that time.

1/8 Unit Load

The RS-485 standard defines both receiver inputs impedance are 12kΩ (1 unit load) and the maximum 32-unit loads on the bus. The PL2303GR transceiver has a 96kΩ input impedance (1/8 unit load) of the receiver, allowing up to 256 or fewer devices to be connected in parallel on the RS-485 bus.

Transmitter Output Protection

The PL2303GR has the current limitation function and the thermal shutdown protection in the transmitter. Firstly, the function of current limitation provides immediate protection against short circuits over the whole common-mode voltage range (-7V to +12V). Secondly, the function of thermal shutdown protection forces the transmitter outputs into a high impedance state if the die temperature becomes excessive.

9. Chip Function Configuration

The default configuration descriptors are stored in the chip internal memory which will be loaded during power-on reset whenever OTPROM is empty. Several of USB configuration descriptors could be modified and programmed one-time into the chip's OTPROM using the PL2303GR OTPROM Writer utility program. These descriptors include Vendor ID, Product ID, Serial Number, Product String, UART settings, GPIO configurations, and other configuration descriptors.

9.1 USB Data Configuration

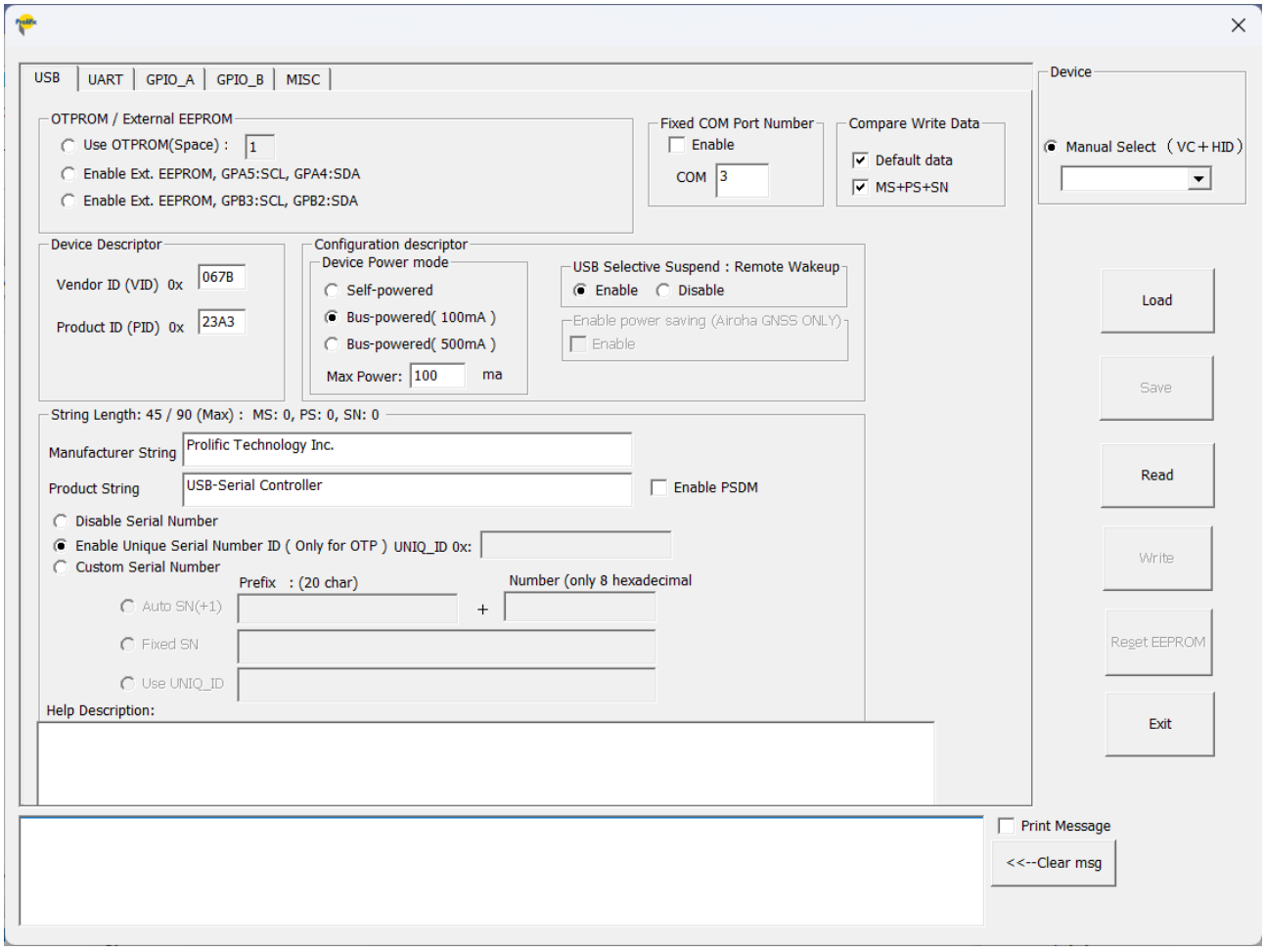


Table 9-1 USB Descriptor Configuration

Descriptors	Default Value	Description
OTPROM	1	This field indicates the space left for the OTPROM that can be written (1 or 0). The OTPROM can only be written once and cannot be erased. If value is 0, it means OTPROM has already been written once.
Vendor ID (VID)	067B (hex)	USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF. Refer to this website for applying VID: http://www.usb.org/developers/vendor/
Product ID (PID)	23A3 (hex)	USB Product ID assigned by Manufacturer.
Device Power Mode	Bus Powered (100mA)	This field sets the USB device if bus-powered or self-powered device.
Max Power	100mA	This field sets the USB device maximum power that can be drawn by the device from the USB host. Enter the value here if it is not 100mA or 500mA. Expressed in 2 mA units (i.e., 50 = 100 mA).
USB Selective Suspend	Enable	This field enables/disables the USB Selective Suspend function. When enabled, Windows OS will suspend the device when idle for few seconds (COM port not open).
Manufacturer String[1]	Prolific Technology Inc.	This field contains the product manufacturer string.

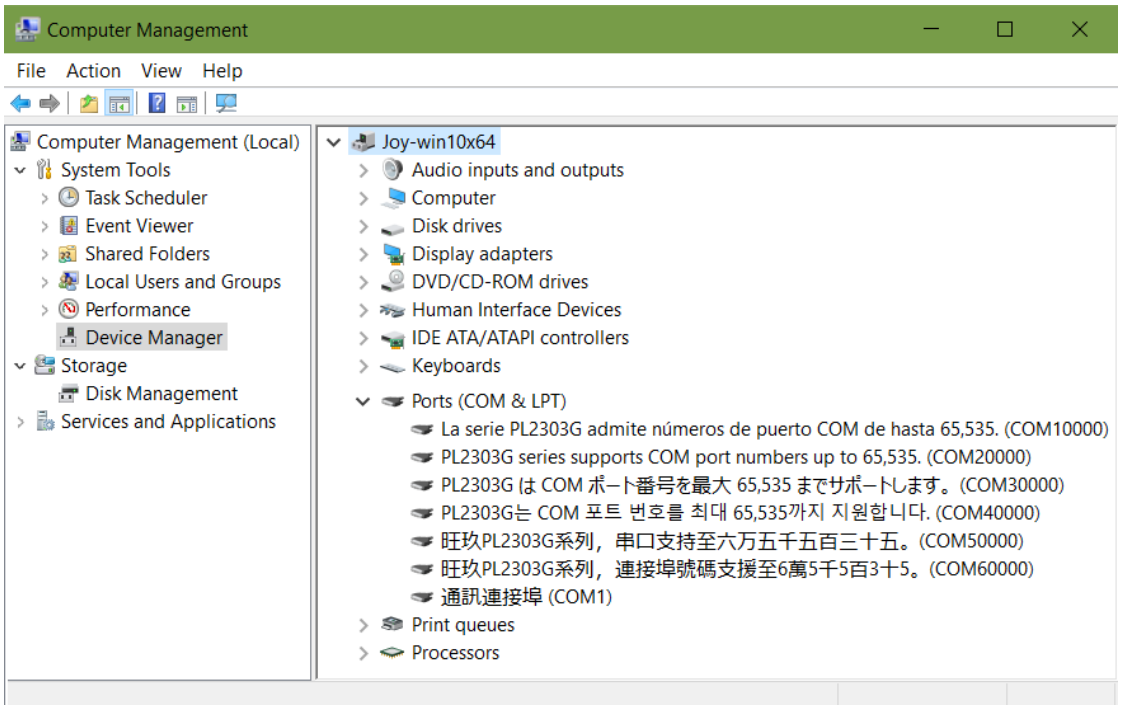
Serial Number[1]	Enable Unique Serial Number ID	• Disable Serial Number – this option will disable the Serial Number. Operating System will assign a random serial number for the device.
		• Enable Unique Serial Number ID – this default option enables the unique serial number pre-programmed inside the chip.
		• Custom Serial Number – this option allows the customer to set own product serial numbering:
		  ○ Auto SN: allows to add prefix while the numbers auto increment after each write.
		  ○ Fixed SN: this will write the same number.
		Device with serial number enabled allows the device to be assigned with the same COM port number even when plug to other USB ports of the same PC.

Product String[1][2]	USB-Serial Controller	When enter wordings(multiple language) in the “Product String” field and check the "Enable PSDM" of OTP tool, the device manager will show the “Product String” entered.
Com Port Number[2]	Disable	Expand COM port number range: from 1~255 to 1~65,535. • When enter the desired COM port number in the "Fixed COM port Number" field and check the "Enable" of OTP tool, the device manager will display the COM port number entered.

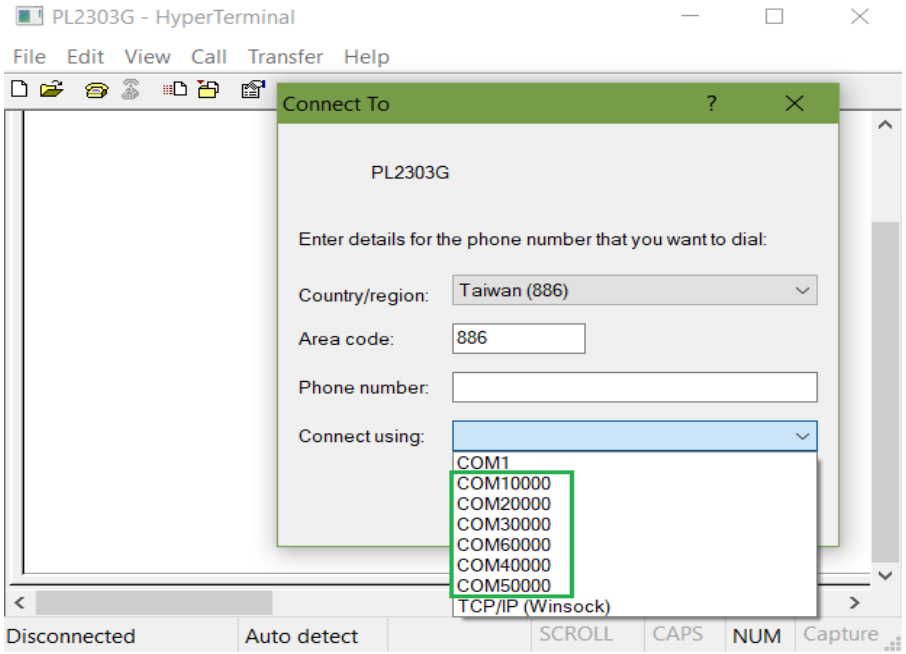
NOTE[1]: The total string length for the manufacturer + serial number + product string is up to 90 characters.

NOTE[2]: How to bind a specific COM port number (1-65,535) and device name(multiple language) via OTP/EEPROM.

Windows Device Manager displays product names in multiple languages.



The HyperTerminal program can connect to high-numbered COM ports. (ex: COM60000)



9.2 RS-485 Configuration

Table 9-2 RS-485 Configuration

Functions	Default Value	Description
LED Flash	Fast	This option sets the flashing speed of the access LED when configured using the TX_LED, RX_LED, TRX_LED GPIO pins. Fast 11.4Hz and slow 2.8Hz.
Remote Wakeup (RXD)	Disable	This allows using the RXD pin as remote wakeup. The received data from RXD may be wrong while chip is waking up.
Software Flow Control	Disable	This option allows setting the software flow control (Xon/Xoff) during chip initial startup. In general, this option need not enabled because driver or software can control this option.
Buffer Size Configuration	256(TX) - 768(RX) 736(HW) - 384(LW)	This sets the internal buffer size configuration for TX (downstream) and RX (upstream) as well as the high and low watermark threshold levels.

9.3 GPIO (GPB) Configuration

Also refer to Section 7.4 for the complete GPIO Multi-Function options description.

Table 9-3 GPIO (GPB Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPB0	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • TX_LED • CLK_OUT[1] (also refer to MISC folder)
GPB1	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • RX_LED • TRX_LED
GPB4	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • CLK_OUT[1] (also refer to MISC folder)
GPB5	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O)
Enable	Disabled		This field sets the selected I/O pin to open-drain output

Open-Drain		mode.
Enable-Pull Up	Disabled	This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to Vo_33. When enabling pull-up for input pins, the input signal voltage should not be higher than the Vo_33 voltage.**
Inverse Polarity	Disabled	This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA	This field sets the output driving strength of the selected pin. (4mA up to 8mA)

[1] **Note: Only one GPIO pin can be configured as CLK_OUT function.**

9.4 Miscellaneous (MISC) Configuration

It includes other miscellaneous chip configuration options including chip I/O suspend state, USB chip suspend, and clock output frequency divider options.

Table 9-4 Miscellaneous Configuration

Functions	Default Value	Description
Suspend Mode I/O State	Keep I/O Driving State	This option allows setting the I/O state when chip is in suspend mode.
USB Chip Suspend	Enabled	This option can enable or disable the USB chip to suspend.
Output Clock Divider	0xFF	This field sets the output clock divider value. When value is 0, output clock pin will stay at low state. When value is 0xff, output clock pin will stay at high state. When other value, output clock rate is 24MHz / (1 + clock divider value). The default value can be kept as is and let customer driver or user tool through SDK to dynamic change the clock divider rate. **Note: Only one GPIO pin can be configured as CLK_OUT function.**

10. Design Application Examples

This section illustrates conceptual design application examples using the PL2303GR.

10.1 USB Bus Powered Design

The PL2303GR has a built-in 3.3V regulator. USB device power (pin VIN) can be supplied directly from USB VBUS pin. The capacitor behind the USB connector on VBUS is a defined requirement of USB specification. If the regulator output VO_33 needs to be maintained at 3.3V, VIN should be larger than 3.6V. It is also recommended to add capacitor at VO_33 pin, please refer to schematic.

This built-in 3.3V regulator can supply the chip operating power around 11mA and also supply the additional 80mA for external components.

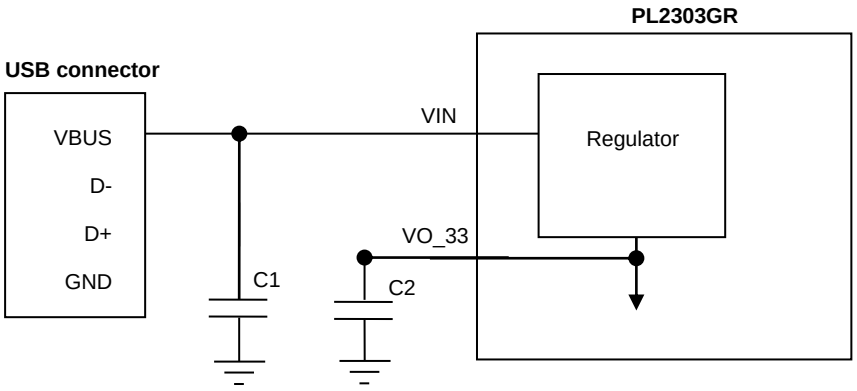


Figure 10-1 USB Bus Powered Design Example

10.2 Chip Reset Control

The PL2303GR has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help system designs to make sure of chip operation start time.

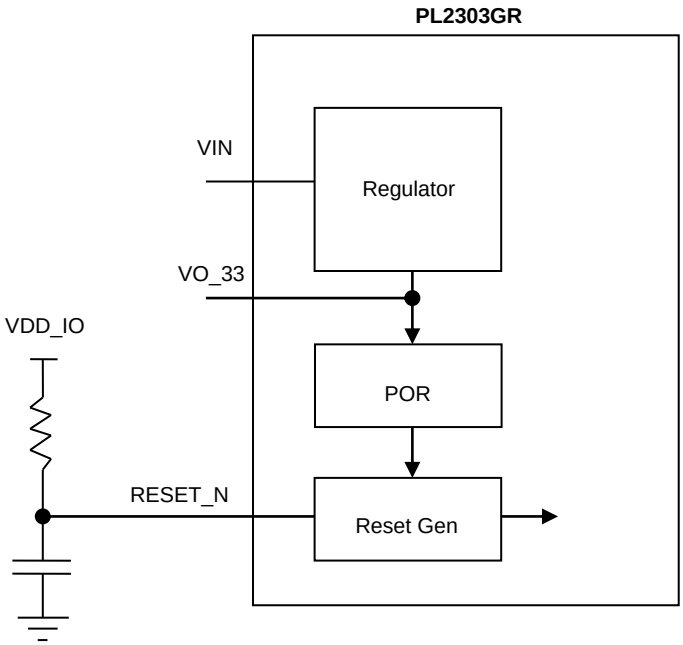


Figure 10-2a Chip Reset Control Application

The power ramp-up time shall keep below than 1ms as shown in diagram below.

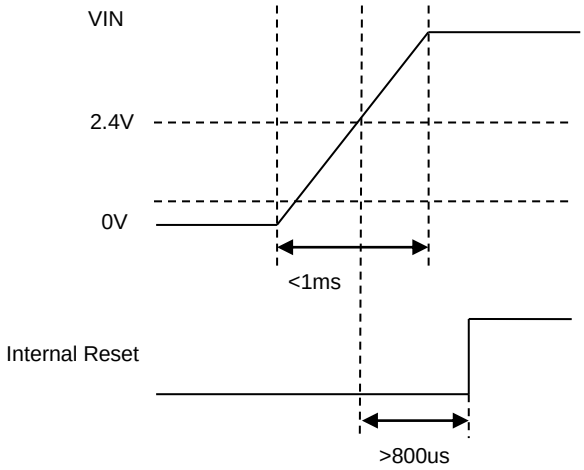


Figure 10-2b Chip Power Reset Timing Diagram

11. DC & Temperature Characteristics

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage – VIN	-0.3 to 6.0 V
Power Supply Voltage – VDD5	-0.3 to 8.0
Receiver Input Voltage –A, B	+-13V
Transmitter Output Voltage	+-13V
Input Voltage of I/O pins with 5V Tolerance I/O	-0.3 to 6.0 V
Storage Temperature	-40 to 150 ^{o}C
Thermal Resistance (θjc)	31 ^{o}C/W (SSOP28)

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

11.2 DC Characteristics

11.2.1 Operating Voltage and Suspend Current

Table 11-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	VIN		5	5.5	V
Power Supply Voltage Range	VDD5		5	5.5	V
Output Voltage of Regulator	VO_33	2.97	3.3	3.63	V
Operating Current(1) (Power Consumption)	I_{DD}	-	10.8		mA
Suspend Current	I_{SUS}	-	650		μA

Note: (1) – No device connected.

11.2.2 I/O Pins

Table 11-2b I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (CMOS)					
Low	V_{IL}	--	--	0.4	V
High	V_{IH}	0.7* VDD_IO	--	--	V
Output Voltage					
Low	V_{OL}	--	--	0.4	V
High	V_{OH}	0.7*VDD_IO	--	--	V

11.3 Temperature Characteristics

Table 11-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

12. Outline Diagram

12.1 Chip Marking information

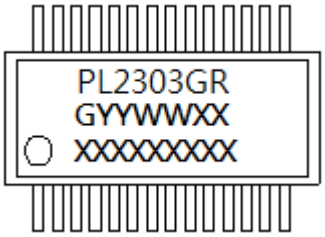


Figure 12-1 Chip Part Number Information (SSOP)

Table 12-2 Chip Marking Information

Line	Marking	Description
First Line	PL2303GR	Chip Product Name
Second Line (GYYWWXX)	G	Green packing material
	YY	Last two digits of the manufacturing year
	WW	Week number of the manufacturing year
	XX	Chip Version
Third Line	XXXXXXXXX	Manufacturing LOT code

Example: "*G19361A*" – means Green packing + Year 2019 + Week no. 36 + 1A chip version.

12.2 SSOP28 Package

Table 12-1 Package Dimension

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
b	0.22		0.38	0.009		0.015
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.021	0.030	0.037
R1	0.09			0.004		
D	9.9	10.2	10.5	0.390	0.402	0.413
A			2.0			0.079
e		0.65			0.0256	
L1		1.25			0.050	
A1	0.05			0.020		
A2	1.65	1.75	1.85	0.065	0.069	0.073

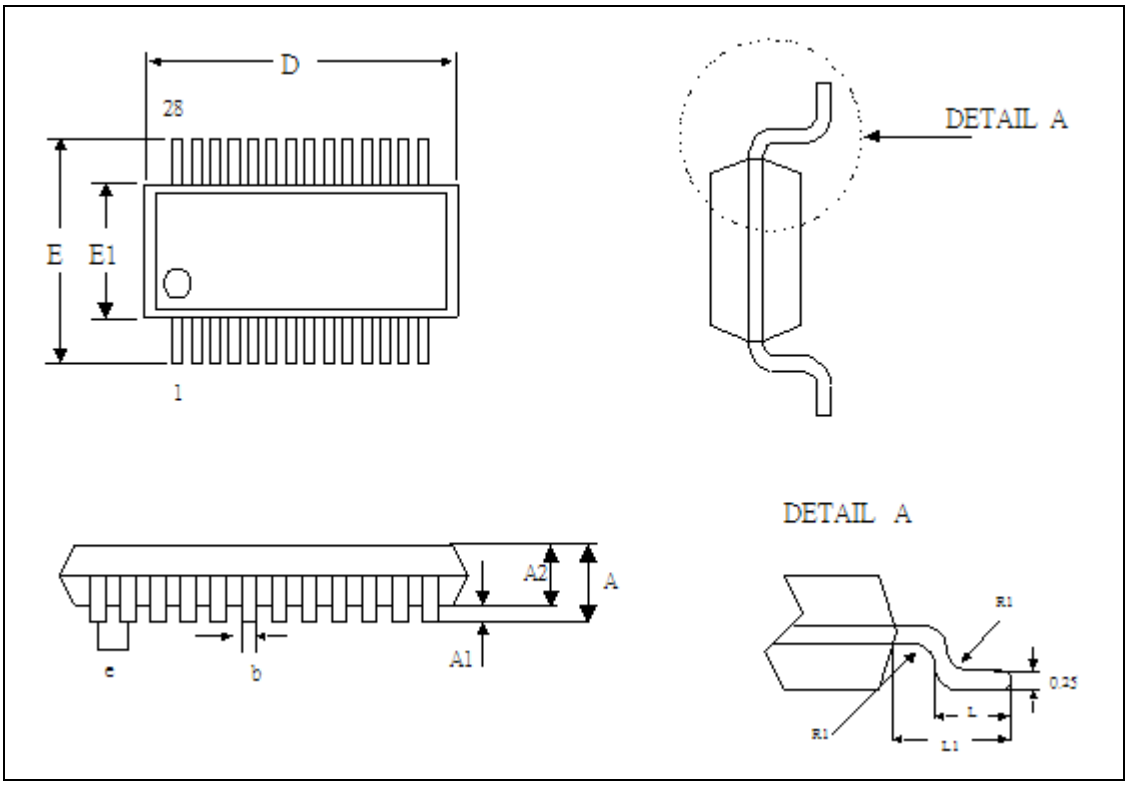


Figure 12-1 PL2303GR Outline Diagram (SSOP28)

13. Packing Information

13.1 Carrier Tape (SSOP-28)

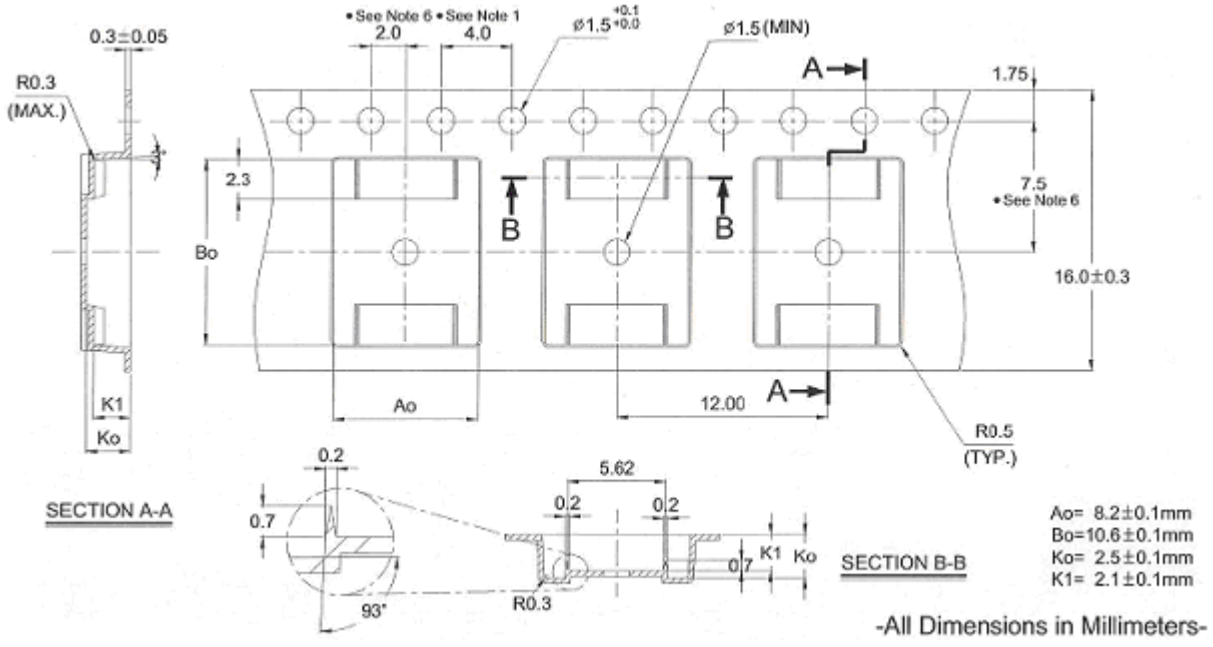


Figure 13-1a SSOP28 Carrier Tape

Notes:

- 10 sprocket hole pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm.
- Material: Black Polystyrene.
- A_o and B_o measured on a plane 0.3mm above the bottom of the pocket.
- K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
- IC quantity per one reel: 2,000 pieces (MOQ)

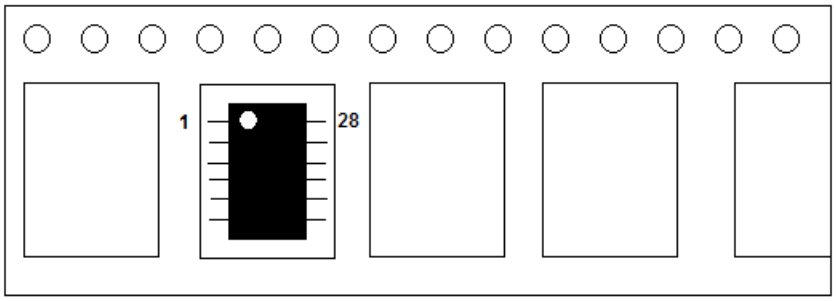


Figure 13-1b IC Reel Placements

13.2 Reel Dimension

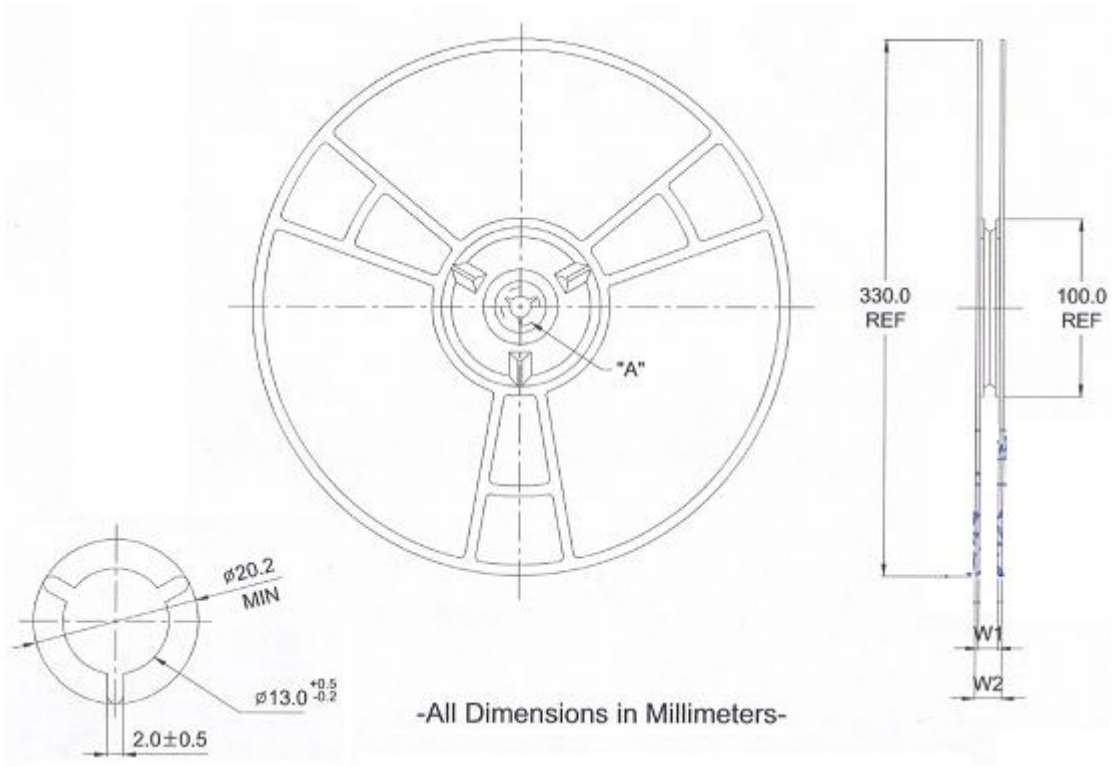


Figure 13-2 Reel Dimension

Table 13-1 Reel Part Number Information

Package	Part Number	Normal Hub Width	W1 +0.3mm -0.2mm	W2 Max
SSOP28	TBD	16mm	16.8mm	22.2mm

13.3 Tube Packing

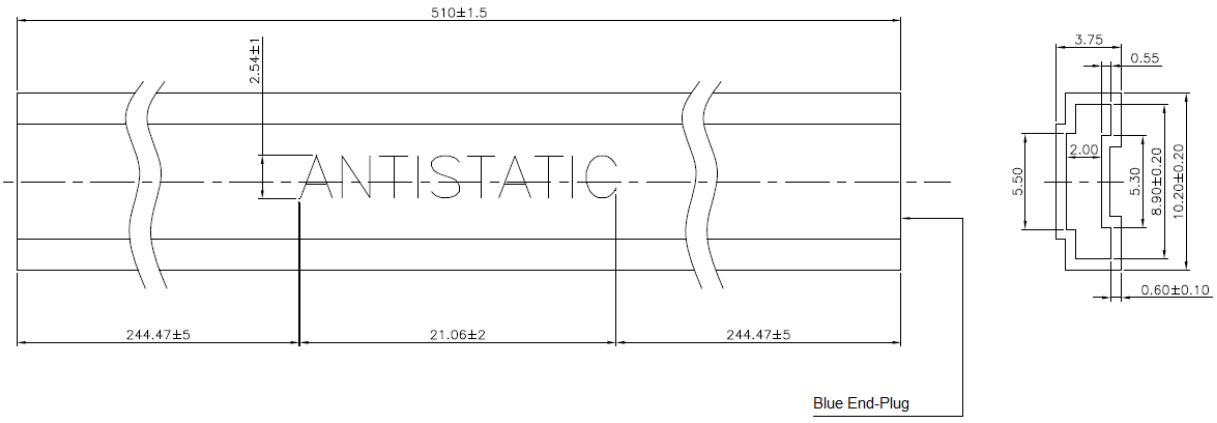


Figure 13-3 Tube Packing Dimension

REMARK :

1.TUBE MT'L : PVC,COATING WITH ANTISTATIE LIQUID.
2.COLOR : TUBE - TRANSPARENT ; MARK - BLUE
3.SURFACE RESISTANCE : 10^{8} ~10^{11} • /□
4.NO BURR AT CUTTING AREA.
5.THE TUBE SHALL WITH BLUE END-PLUG(3088-060-01681) FROM VENDOR, TAIL DOWNWARD AND THE OTHER ONE ENCLOSE TOGETHER WITH SHIPMENT.

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