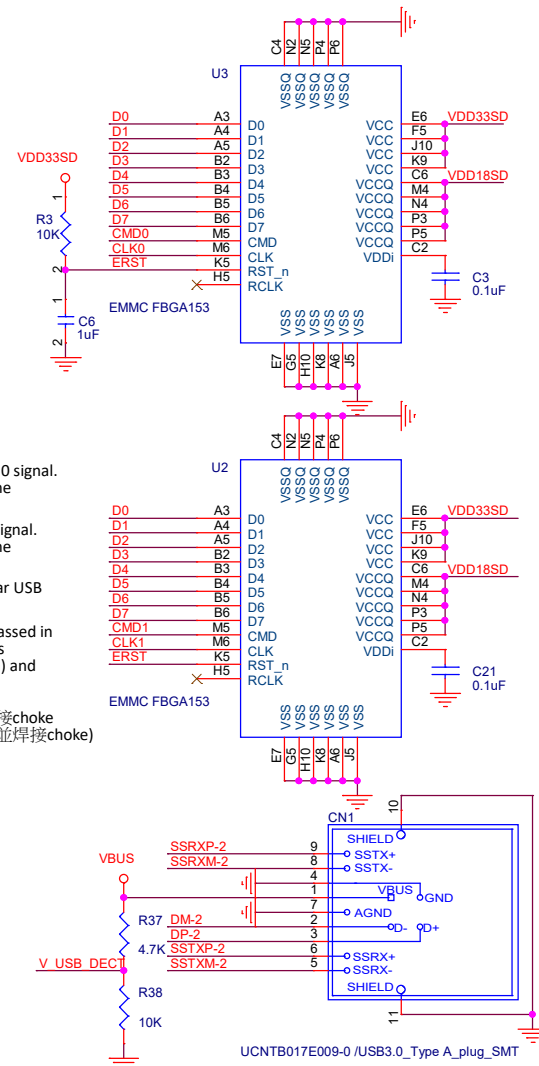
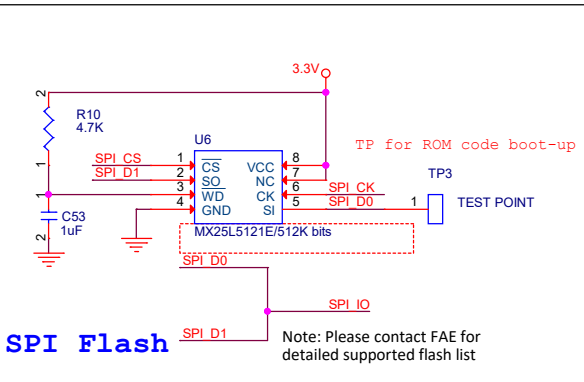


Note:

- Optional L2, L3 for reducing EMI of USB3.0 signal. The impedance of the choke depends on the impedance of USB3.0 trace on PCB
- Optional L4 for reducing EMI of USB2.0 signal. The impedance of the choke depends on the impedance of USB2.0 trace on PCB
- C2, C4, L2, L3, L4 should be placed as near USB connectors as possible
- L2~L3 do not be applied because they are bypassed in the schematic. If PCBA can't pass for EMI test, it is needed to cut the bypass trace (for short of them) and apply them for EMI reduction.
(因不一定需要choke才能通過EMI認證，故此電路已先將CM choke旁路，EMI初測時不需焊接choke，若EMI無法通過測試，再將旁路的走線割除並焊接choke)



Note
To prevent from the cross routing of SSTX+ and SSTX- (or SSRX+ and SSRX-) between USB connector and PL2733 while doing PCB layout, SSTX+ and SSTX- (or SSRX+ and SSRX-) of PL2733 can be swapped and then connected to a USB connector.
(PCB layout時，為了避免 SSTX+ 及 SSTX- (或 SSRX+ 及 SSRX-) 出現交叉佈線，PL2733的這兩組信號的同一組正及負信號可對調連接到USB連接器)



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