
Product Data Sheet**PL2732**

1. Features

- Single-chip SuperSpeed USB 3.0 Storage Controller Solution
- Compliant with USB 3.0 and USB 2.0 specification
- Integrated SuperSpeed (5Gbps), Hi-Speed, and Full-speed USB transceiver
- Supports high-performance 8-bit eMMC of BGA package (up to eMMC 5.0 HS200 speed grade)
- JBOD capability combines dual storage media capacity into one high-capacity USB drive
- Embedded high-performance microcontroller
- Supports USB Mass Storage Class (MSC) and Bulk-Only Transport Specification. No device driver installation needed for major Operating Systems (Windows, Mac, Linux, and Android).
- Firmware can be upgraded via USB interface using either external SPI flash or storage media (to further reduce PCB footprint and BOM cost)
- Built-in eMMC power regulator
- Built-in 5V to 3.3V regulator
- Built-in 5V to core voltage regulator
- LQFP48 package

2. General Description

The PL2732 is a single-chip SuperSpeed USB 3.0 eMMC storage controller with protocol engine that provides USB 3.0 to 8-bit eMMC interface for PCs/tablets/smartphones. When connected to the SuperSpeed USB port of PC, the PL2732 activates its USB BOT Mass Storage Class protocol engine and transfers files at USB 3.0 SuperSpeed (5Gbps) that enables the eMMC media up to HS200 performance grade. The PL2732 uses OS built-in USB mass storage drivers so no driver installation is needed for major operating systems like Windows, Mac, Linux, and Android. The PL2732 can be configured as a single LUN USB drive using either one or two storage media. The PL2732 incorporates JBOD capability that provides the flexibility to use two storage media and combine their capacity into one logical drive.

To save BOM cost, the PL2732 integrates both SuperSpeed transceiver and Hi-Speed/Full-speed transceiver. It also integrates power management components including eMMC power regulator and other regulators. It also integrates chip power stability monitors to make sure the controller does not enter unknown state when system power is unstable. To maximize system compatibility and to integrate more value-added features, the firmware of PL2732 can also be upgraded via USB interface and stored in the external SPI flash.

3. Block Diagram

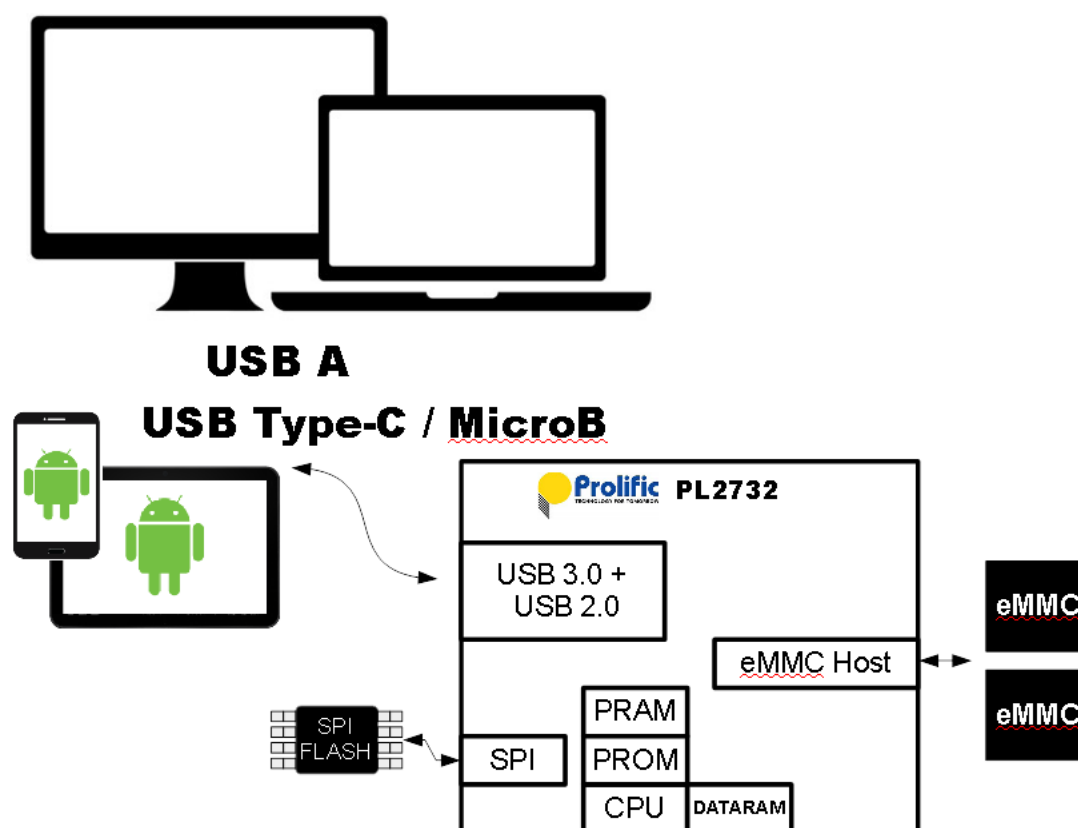


Figure 3-1: PL2732 Block Diagram & Application

4. Ordering Information

Table 4-1: Ordering Information

Product Name	Package Type	Ordering Number
PL2732	48pin LQFP (7x7mm)	PL2732B4LMG7P1(*1)

(*1) This packaging is applicable to MSL 3 (Based on IPC/JEDEC J-STD-020) for MPQ (Minimum Package Quantity)

Table of Contents

1. Features.....1

2. General Description.....1

3. Block Diagram.....2

4. Ordering Information.....2

5. Pin Assignment & Description5

 5.1 PL2732 Pin Assignment.....5

 5.2 PL2732 Pin Description Table6

6. AC & DC Characteristics8

 6.1 Absolute Maximum Ratings8

 6.2 Recommended Operating Conditions8

 6.3 Operating Current.....8

 6.4 Signal level of SD(eMMC) bus.....9

7. Package Outline Diagram10

 7.1 Chip Marking information.....10

 7.2 Outline Diagram..... 11

List of Figures

Figure 3-1: PL2732 Block Diagram & Application..... 2

Figure 5-1: PL2732 Pin Diagram 5

Figure 7-1: PL2732 Outline Diagram (LQFP48 7x7mm) 11

List of Tables

Table 4-1: Ordering Information..... 2

Table 5-1: PL2732 Pin Assignment..... 6

Table 6-1: Absolute Maximum Ratings..... 8

Table 6-2: Recommended Operating Conditions..... 8

Table 6-3 Operating Current..... 8

Table 6-4: Signal level of SD bus at VDDIOSD=3.3V..... 9

Table 6-5: Signal level of SD bus at VDDIOSD=1.8V..... 9

5. Pin Assignment & Description

5.1 PL2732 Pin Assignment

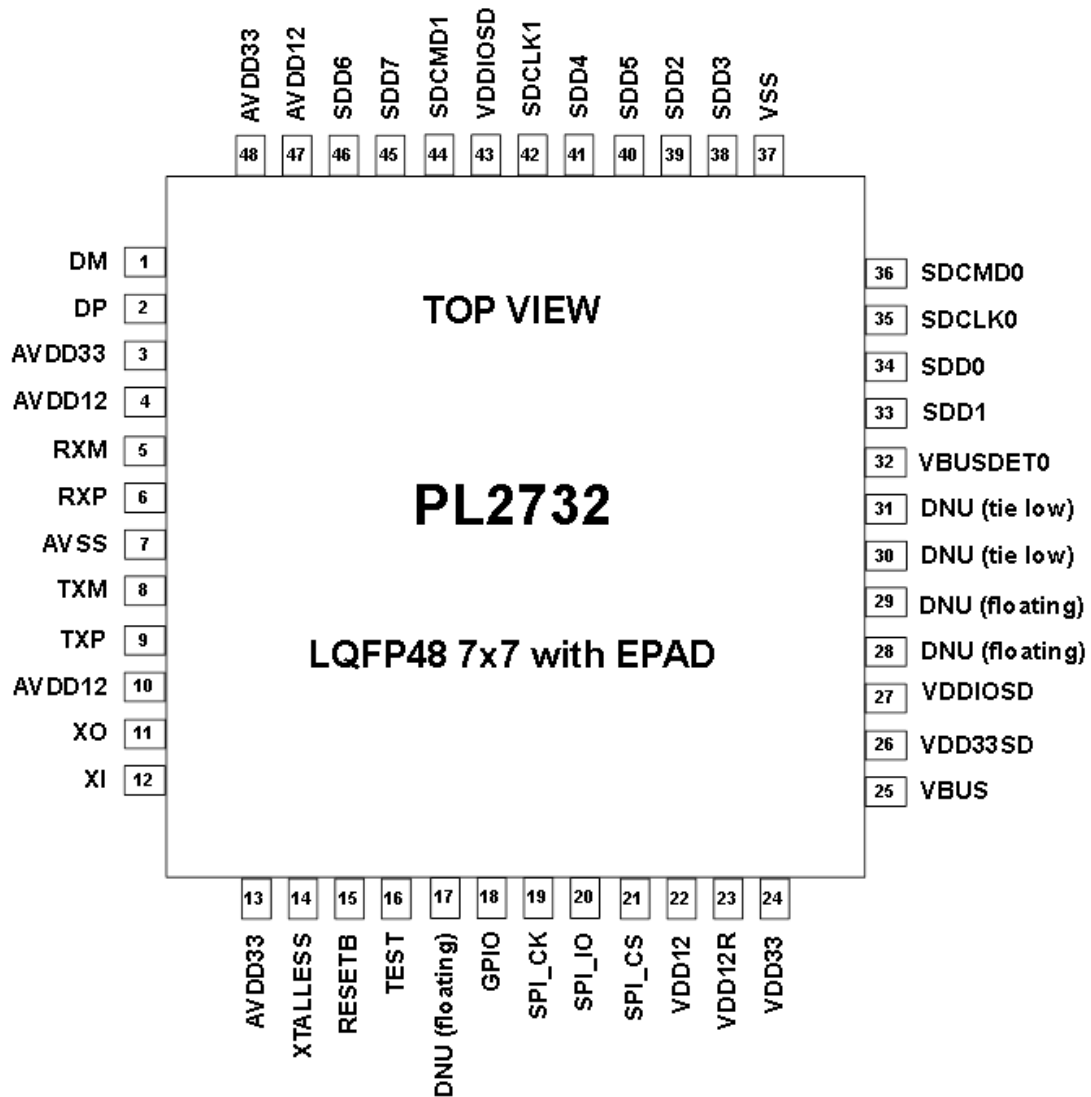


Figure 5-1: PL2732 Pin Diagram

5.2 PL2732 Pin Description Table

Table 5-1: PL2732 Pin Assignment

Pin #	Pin Name	Pin Type	Pin Description
1	DM	AIO	USB DM
2	DP	AIO	USB DP
3	AVDD33	P	3.3V Analog Power
4	AVDD12	P	1.2V Analog Power
5	RXM	AIO	USB SuperSpeed RXM
6	RXP	AIO	USB SuperSpeed RXP
7	AVSS	P	Analog Ground
8	TXM	AIO	USB SuperSpeed TXM
9	TXP	AIO	USB SuperSpeed TXP
10	AVDD12	P	1.2V Analog Power
11	XO	DO	30MHz Crystal Oscillator Output
12	XI	DI	30MHz Crystal Oscillator Input
13	AVDD3	P	3.3V Analog Power
14	XTALLESS	DI	High: clock from internal oscillator Low: clock from external crystal
15	RESETB	DI	Active low reset
16	TEST	DI	Active high test mode. Tie this pin to ground.
17	DNU	-	Do not use. Leave this pin floating.
18	GPIO	DIO	Do not use. Leave this pin floating.
19	SPI_CK	DO	SPI Clock
20	SPI_IO	DIO	SPI Data
21	SPI_CS	DO	SPI Chip Select
22	VDD12	P	1.2V Power
23	VDD12R	P	1.2V output power (internal regulator)
24	VDD33	P	3.3V output power (internal regulator)
25	VBUS	P	USB VBUS
26	VDD33SD	P	3.3V output power for eMMC Max output current: 250mA Output Voltage range: 3.3V +/- 5%
27	VDDIOSD	P	Power for eMMC IO Interface
28	DNU	DIO	Do not use. Leave this pin floating.
29	DNU	-	Do not use. Leave this pin floating.
30	DNU (tie low)	DIO	Do not use. Tie this pin to GND.
31	DNU (tie low)	DI	Do not use. Tie this pin to GND.

32	VBUSDET0	DI5VT	VBUS detection 0
33	SDD1	DIO	Data bit 1 of eMMC
34	SDD0	DIO	Data bit 0 of eMMC
35	SDCLK0	DO	Clock pin of eMMC #0
36	SDCMD0	DIO	CMD pin of eMMC #0
37	VSS	P	VSS
38	SDD3	DIO	Data bit 3 of eMMC
39	SDD2	DIO	Data bit 2 of eMMC
40	SDD5	DIO	Data bit 5 of eMMC
41	SDD4	DIO	Data bit 4 of eMMC
42	SDCLK1	DO	Clock pin of eMMC #1
43	VDDIOSD	P	Power for IO of eMMC
44	SDCMD1	DIO	CMD pin of eMMC #1
45	SDD7	DIO	Data bit 7 of eMMC
46	SDD6	DIO	Data bit 6 of eMMC
47	AVDD12	P	1.2V Analog Power
48	AVDD33	P	3.3V Analog Power
49	EPAD	EPAD	VSS

Pin Type:

- AIO – Analog Bi-directional
- P – Power / Ground
- DI – Digital Input
- DO – Digital Output
- DIO – Digital Bi-directional
- DI5VT – Digital Input, 5V Tolerant

6. AC & DC Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{BUS}	Power supply of VBUS	-0.3 to 5.5	V
V _{DD12}	Power supply of 1.2V (VDD12, AVDD12)	-0.3 to 1.31	V
V _{DD33}	Power supply of 3.3V (VDD33, AVDD33)	-0.3 to 3.6	V
V _{IN33}	Input signal voltage of 3.3V IO	-0.3 to 3.6	V
V _{ESD-MM}	Machine Mode	±300	V
V _{ESD-HBM}	Human Body Mode	±4	KV
T _{op}	Operating temperature	-40 to 85	°C
T _J	Junction Operation Temperature	-40 to 125	°C
T _{STG}	Storage temperature	-40 to 150	°C

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{BUS}	Power supply of VBUS	2.7		5.5	V
V _{DD12}	Power supply of 1.2V (VDD12, AVDD12)	1.28		1.31	V
V _{DD33}	Power supply of 3.3V (VDD33, AVDD33)	2.7	3.3	3.6	V
V _{DI5VT}	Voltage of 5V tolerance pin	2.7		5.5	V

6.3 Operating Current

The current is measured from VBUS pin of USB connector and the condition applies the external crystal, the external power supply of 1.2V and FORESEE 32GB eMMC memory. The operating current varies during write and read operation and the current mainly depends on the power consumption of eMMC memory.

Table 6-3 Operating Current

Symbol	Parameter	Condition	Current #1	Current #2	Units
I _{OP}	Operating Current	USB 3.0	80 ~115(*1)	75~105(*2)	mA
		USB 2.0	70~85(*1)	50~65(*2)	mA
I _{IDLE}	Idle Current	USB 3.0	52	N/A	mA
		USB 2.0	24	N/A	mA
I _{SUS}	Suspend Current	USB 3.0	2	N/A	mA
		USB 2.0	2	N/A	mA

*1: The **write current** is measured during the files are written to PL2732 disk.

*2: The **read current** is measured during the files are read from PL2732 disk.

6.4 Signal level of SD(eMMC) bus

To meet the requirements of the JEDEC specification JESD8-1A, the input and output voltages of the bus shall be within the following specified ranges.

Table 6-4: Signal level of SD bus at VDDIOSD=3.3V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{IH}	Input High Voltage	2.063		3.6	V
V _{IL}	Input Low Voltage	-0.3		0.825	V
V _{OL}	Output Low Voltage			0.4125	V
V _{OH}	Output High Voltage	2.475			V

Table 6-5: Signal level of SD bus at VDDIOSD=1.8V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{IH}	Input High Voltage	1.125		2.1	V
V _{IL}	Input Low Voltage	-0.3		0.45	V
V _{OL}	Output Low Voltage			0.225	V
V _{OH}	Output High Voltage	1.35			V

7. Package Outline Diagram

7.1 Chip Marking information



Table 7-1 Chip Marking Information

Line	Marking	Description
First Line	PL2732	Chip Product Name
Second Line (GYYWWXX)	G	Green packing material
	YY	Last two digits of the manufacturing year
	WW	Week number of the manufacturing year
	XX	Chip Version
Third Line	XXXXXXXXXX	Manufacturing LOT code

Example: "G24424B" – means Green packing + Year 2024 + Week no. 42 + 4B chip version.

7.2 Outline Diagram

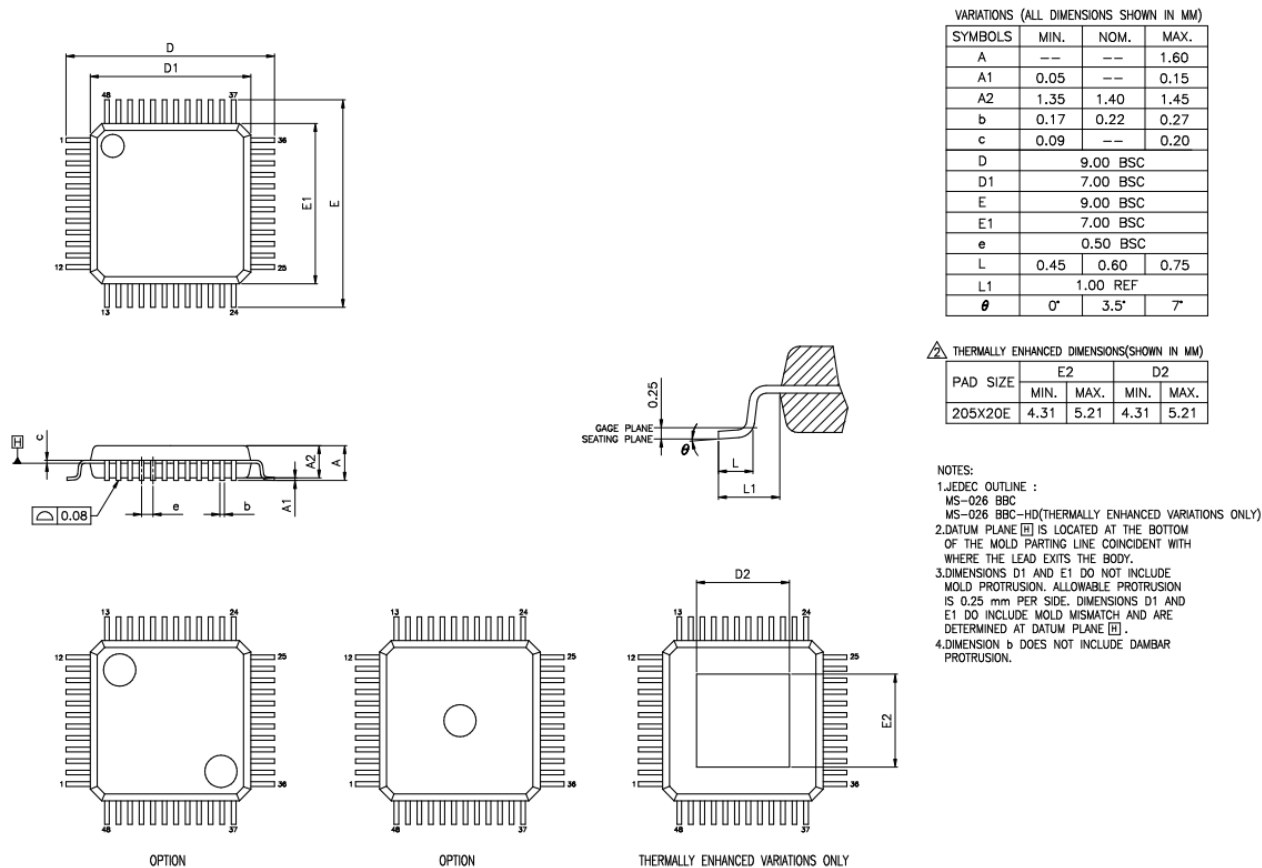


Figure 7-1: PL2732 Outline Diagram (LQFP48 7x7mm)

Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Trademarks

The Prolific logo is a registered trademark of Prolific Technology Inc. All brand names and product names used in this document are trademarks or registered trademarks of their respective holders.

Copyrights

Copyright © 2016-2025 Prolific Technology Inc. All rights reserved.

No part of this document may be reproduced or transmitted in any form by any means without the express written permission of Prolific Technology Inc.

Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.

Nan Kang, Taipei 115, Taiwan, R.O.C.

Telephone: +886-2-2654-6363

Fax: +886-2-2654-6161

E-mail: sales@prolific.com.tw

Website: <http://www.prolific.com.tw>