USB 3.0 iOS/Generic Storage Controller

Product Data Sheet PL2733

1. Features

- Single-chip SuperSpeed USB 3.0 Storage Controller Solution
- Compliant with USB 3.0 and USB 2.0 specification
- Integrated SuperSpeed (5Gbps), Hi-Speed, and Full-speed USB transceiver
- High-performance embedded microcontroller
- Dual-protocol engine to support both Apple® iOS devices (tablets/smartphones) and major Operating Systems (Windows, Mac, Linux, Android) for systems/tablets/smartphones
- Supports mainstream cost-efficient storage media: Secure Digital™ card (SDSC, SDHC, SDXC, up to v3.01 UHS-I SDR104 and compliant with SD5.0 UHS-II SD card) and MultiMediaCard™ (MMC) up to v4.2
- Supports high-performance eMMC of BGA package (up to eMMC 5.0 HS200)
- JBOD capability combines dual storage media capacity into one big capacity USB drive
- Supports USB Mass Storage Class (MSC) Bulk-Only Transport Specification. No device driver installation needed.
- Firmware can be upgraded via USB interface using either external SPI flash or storage media (to further reduce PCB footprint and BOM cost)
- Built-in SD card power regulator
- Built-in SD UHS interface power regulator
- Built-in 5V to 3.3V GPIO regulator
- Built-in 5V to core voltage regulator
- QFN48 small-size package
- I2C interface to communicate with Apple® authentication co-processor

2. General Description

The PL2733 is a single-chip SuperSpeed USB 3.0 storage controller with dual-protocol engine that provides Lightning and USB 3.0 to SD/MMC/eMMC interface for Apple iOS tablet/smartphone devices and for PCs/tablets/smartphones based on major operating systems like Windows, Mac, Linux, and Android. When plugged to the Lightning connector of Apple® iOS devices, the PL2733 activates the Apple® protocol engine to fully utilize the bandwidth of Apple® proprietary connector and also maintain low power consumption. When plugged into the PC SuperSpeed USB host, the PL2733 activates its USB BOT Mass Storage Class protocol engine and transfers files at USB 3.0 SuperSpeed rate of 5Gbps to/from SD cards. The PL2733 uses OS built-in USB mass storage drivers so no driver installation is needed. The PL2733 can also be configured as a single LUN USB drive using one or two storage media. The PL2733 incorporates JBOD capability that allows you the flexibility to use two storage media and combine their capacity into one fixed logical drive USB flash drive solution.

To save BOM cost, the PL2733 integrates both SuperSpeed transceiver and Hi-Speed/Full-speed transceiver. It also integrates power management components including SD card power regulator, SD interface regulator, and GPIO regulator. It also integrates chip power stability monitors to make sure controller does not enter unknown state when system power is unstable. To maximize system compatibility and to integrate more value-added features, the PL2733 can also be upgraded through commodity SPI flash.

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3. Block Diagram

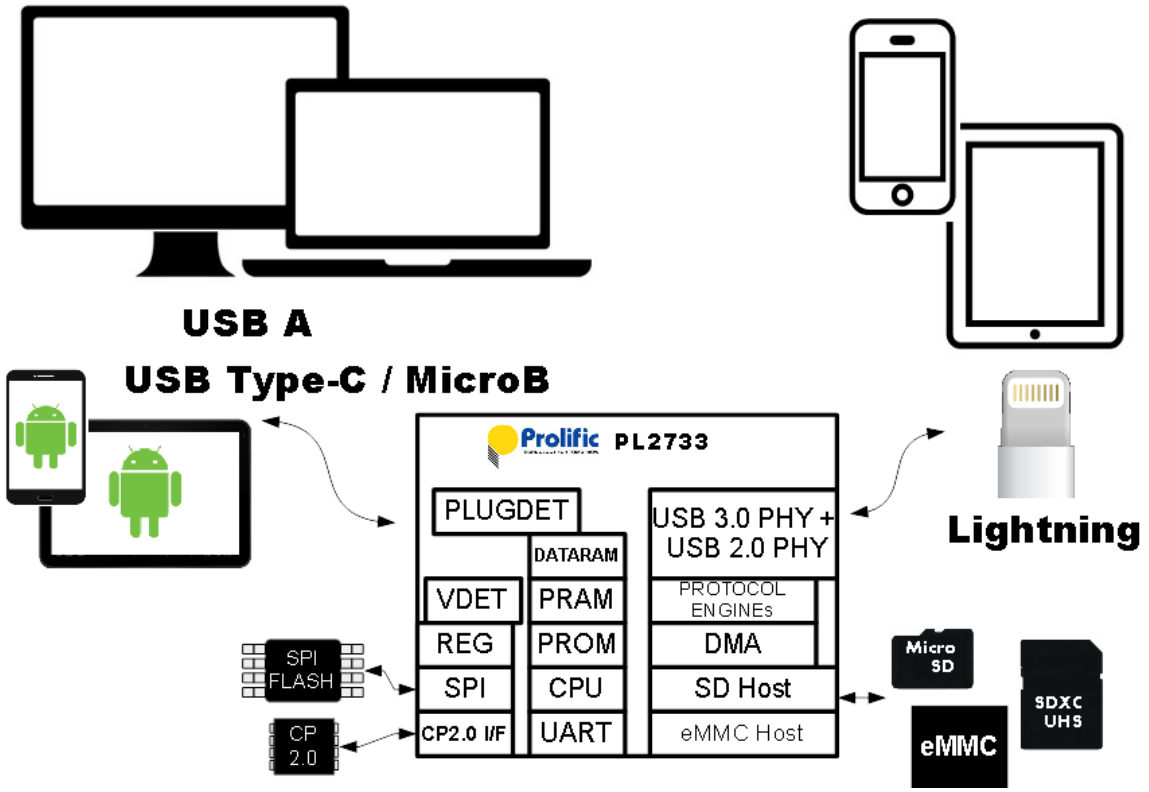

Figure 3-1: PL2733 Block Diagram & Application

4. Ordering Information

Table 4-1: Ordering Information

Product Name	Package Type	Ordering Number
PL2733	48pin QFN (7x7mm)	*TBD*

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5. Pin Assignment & Description

5.1 PL2733 Pin Assignment

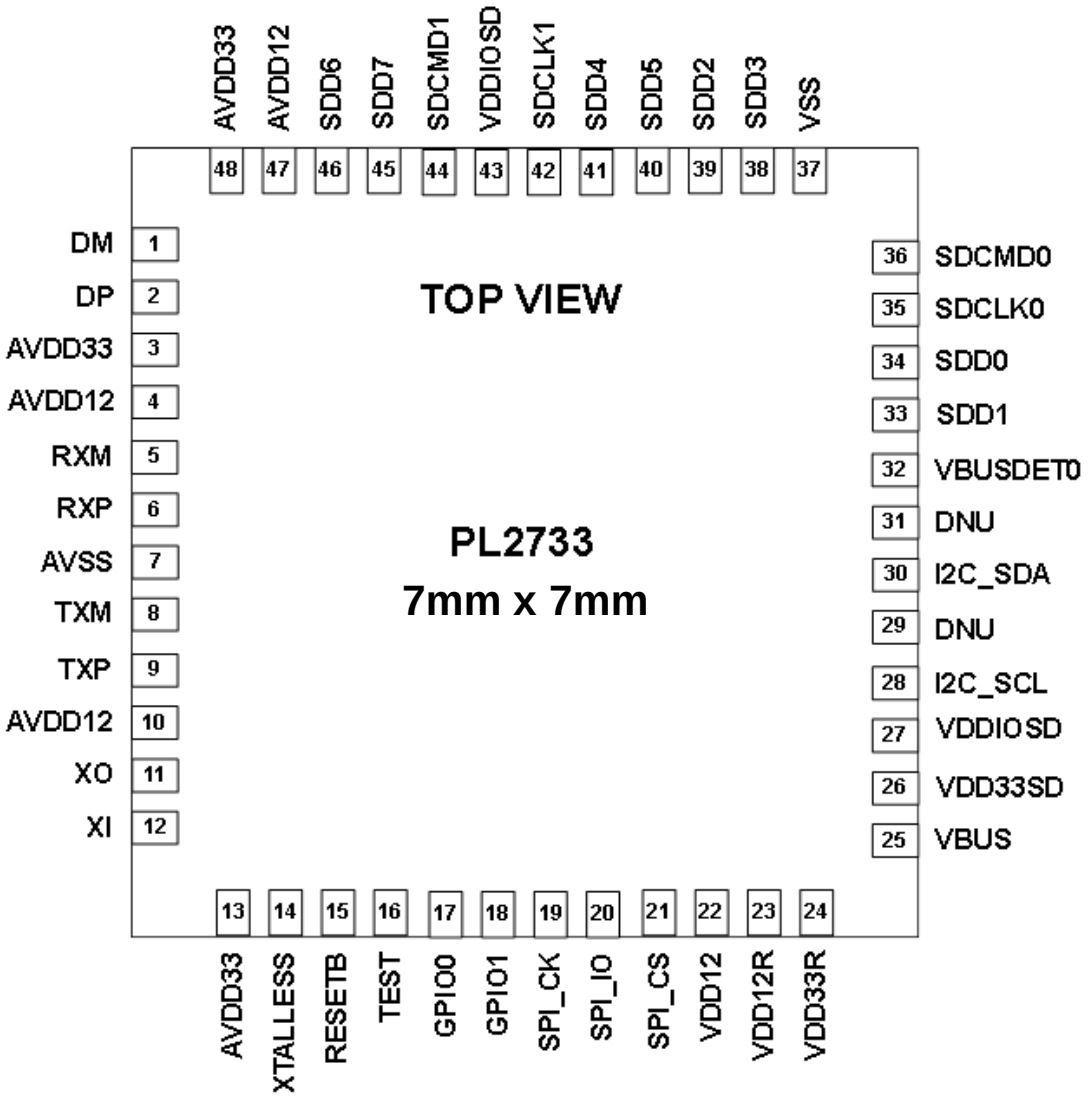


Figure 5-1: PL2733 Pin Diagram

5.2 PL2733 Pin Description Table

Table 5-1: PL2733 Pin Assignment

Pin #	Pin Name	Pin Type	Pin Description
1	DM	AIO	USB DM
2	DP	AIO	USB DP
3	AVDD33	P	3.3V Analog Power
4	AVDD12	P	1.2V Analog Power
5	RXM	AIO	USB SuperSpeed RXM
6	RXP	AIO	USB SuperSpeed RXP
7	AVSS	P	Analog Ground
8	TXM	AIO	USB SuperSpeed TXM
9	TXP	AIO	USB SuperSpeed TXP
10	AVDD12	P	1.2V Analog Power
11	XO	DO	30MHz Crystal Oscillator Output
12	XI	DI	30MHz Crystal Oscillator Input
13	AVDD3	P	3.3V Analog Power
14	XTALLESS	DI	Tie this pin to ground through 0-Ohm resistor
15	RESETB	DI	Active low reset
16	TEST	DI	Active high test mode. Tie this pin to ground.
17	GPIO0	DIO	GPIO
18	GPIO1	DIO	GPIO
19	SPI_CK	DO	SPI Clock
20	SPI_IO	DIO	SPI Data
21	SPI_CS	DO	SPI Chip Select
22	VDD12	P	1.2V Power
23	VDD12R	P	Reserved.
24	VDD33R	P	3.3V Power output
25	VBUS	P	Power input from USB connector
26	VDD33SD	P	3.3V Power output for SD Card. Max output current: 250mA Output Voltage range:3.3V+/- 5%
27	VDDIOSD	P	Power output for SD Interface IO
28	I2C_SCL	DIO	I2C SCL
29	DNU	-	Do not use. Leave this pin floating.
30	I2C_SDA	DIO	I2C SDA
31	DNU	-	Do not use. Leave this pin floating.
32	VBUSDET0	DI5VT	VBUS detection 0

33	SDD1	DIO	Data bit 1 of SD card 0
34	SDD0	DIO	Data bit 0 of SD card 0
35	SDCLK0	DO	Clock pin of SD card 0
36	SDCMD0	DIO	CMD pin of SD card 0
37	VSS	P	VSS
38	SDD3	DIO	Data bit 3 of SD card 0
39	SDD2	DIO	Data bit 2 of SD card 0
40	SDD5	DIO	Data bit 1 of SD card 1
41	SDD4	DIO	Data bit 0 of SD card 1
42	SDCLK1	DO	Clock pin of SD card 1
43	VDDIOSD	P	Power for IO of SD interface
44	SDCMD1	DIO	CMD pin of SD card 1
45	SDD7	DIO	Data bit 3 of SD card 1
46	SDD6	DIO	Data bit 2 of SD card 1
47	AVDD12	P	1.2V Analog Power
48	AVDD33	P	3.3V Analog Power
49	EPAD	EPAD	VSS

Pin Type:

- AIO – Analog Bi-directional
- DI – Digital Input
- DIO – Digital Bi-directional
- P – Power / Ground
- DO – Digital Output
- DI5VT – Digital Input, 5V Tolerant

6. AC & DC Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{BUS}	Power supply of VBUS	-0.3 to 5.5	V
V_{DD12}	Power supply of 1.2V (VDD12, AVDD12)	-0.3 to 1.31	V
V_{DD33}	Power supply of 3.3V (VDD33, AVDD33)	-0.3 to 3.6	V
V_{IN33}	Input signal voltage of 3.3V IO	-0.3 to 3.6	V
V_{ESD-MM}	Machine Mode	±300	V
$V_{ESD-HBM}$	Human Body Mode	±4	KV
T_{op}	Operating temperature	0 to 70	^{o}C
T_{STG}	Storage temperature	-40 to 150	^{o}C

6.2 Operating Current

Table 6-2: Operating Current Parameters

Symbol	Parameter	Min	Typ	Max	Units
I_{DD1}	Normal mode current			TBD	mA
I_{DD2}	Low power mode current			TBD	mA

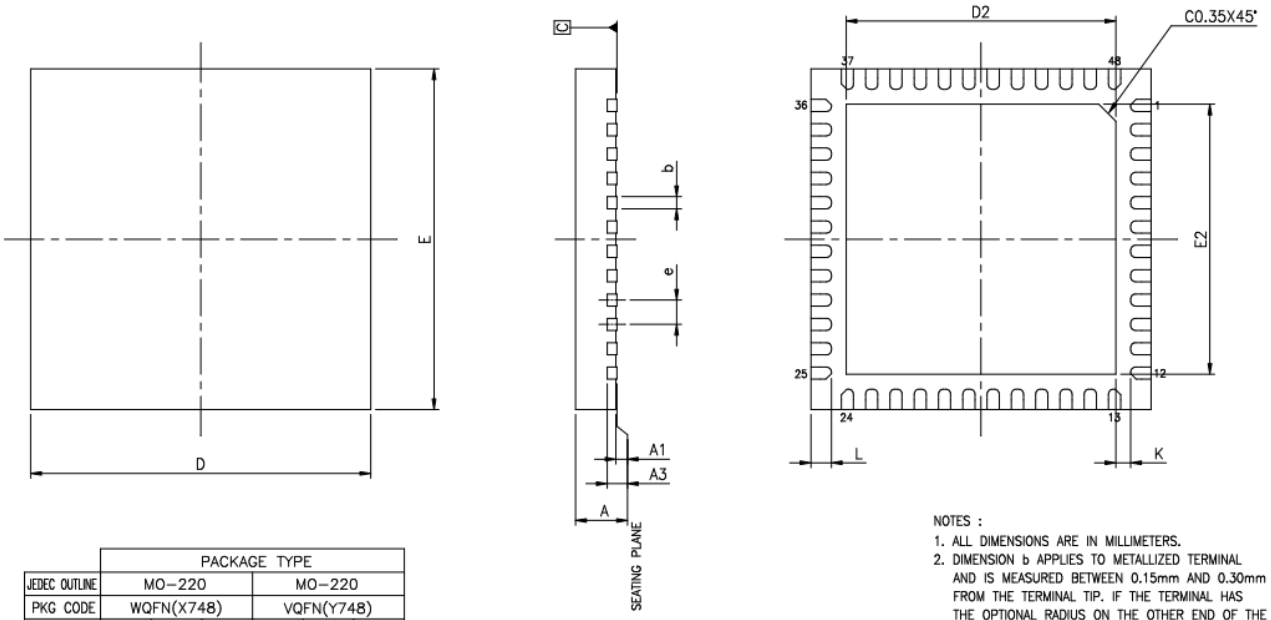
6.3 Recommended Operating Conditions

Table 6-3: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{BUS}	Power supply of VBUS	2.7		5.5	V
V_{DD12}	Power supply of 1.2V (VDD12, AVDD12)	1.25	1.28	1.31	V
V_{DD33}	Power supply of 3.3V (VDD33, AVDD33)	2.7	3.3	3.6	V
V_{DI5VT}	Voltage of 5V tolerance pin	2.7		5.5	V

7. Package Outline Diagram

7.1 Outline Diagram



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X748)			VQFN(Y748)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30
D	7.00 BSC			7.00 BSC		
E	7.00 BSC			7.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

	D2			E2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.20	5.30	5.40	5.20	5.30	5.40	0.35	0.40	0.45	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 7-1: PL2733 Outline Diagram (QFN48 7x7mm)

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