Product Data Sheet **PL2543**

PL2543 USB 2.0 to 4-port Full UART Controller

USB Interface

- Fully compliant with USB 2.0 specification
- USB-IF certified TID 6180
- UHCI/OHCI (USB1.1), EHCI (USB2.0), and Xhci (USB3) host controller compatible
- USB CDC driver and SDK:
  - Using built-in CDC driver on Win10(* 1), Mac OS X 10.7, Linux 3.8, Android 3.2 and their later version.
  - Provides USB CDC-to-UART SDK for Mac OS X, Linux, and Android and SDK of virtual-com-port for Windows.
- Royalty-free USB to Virtual COM Port drivers for Windows, Mac, Linux, and Android
- Highly integrated USB 2.0 High-Speed and Full-speed transceiver with built-in pull-up resistor and reference resistor to reduce PCB external component
- Support on-chip MTP for customization of USB device, configuration, and serial number descriptors, no need of external memory
- Each IC has unique ID (for serial number)
- Support bus-powered, self-powered and high-power USB configuration
- Support Windows USB selective suspend (remote wakeup enabled)
- Support VBUS detect function to attach USB host after VBUS is detected

*1 . Default using Prolific virtual-com-port driver on Win7&8

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-IO functions
- Configurable output driving strength
- Total 11 GPIOs can be used
- Optional clock output and PWM output
- Flexible GPIO configuration
- HBM ±6.0KV ESD protection
- MM ±300V ESD protection
- Latch up ±200mA protection

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Product Data Sheet PL2543

UART Interface

- Support 4-port full UART interface
  - Individual 4-port full UART interface
  - RS232, RS422, RS485
  - Flexible baud rate support from 5 bps to 24M bps
  - 5, 6, 7, or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and half, or two stop bits
  - Hardware flow control (CTS/RTS and/or DSR/DTR)
  - Software flow control (XON/XOFF)
  - Configurable remote wakeup pin
- Individual 512bytes FIFO for IN/OUT buffer per port
- Configurable threshold of flow control
- Configurable transmit and receive LED pins
- Configurable invert option of UART signals
- Suspend pin control for RS232 transceiver

Miscellaneous

- Integrated Power-on-Reset (POR) circuit
- Integrated 5V to 3.3V LDO that can support 100mA for chip internal or external components
- Independent and wide I/O voltage range (+1.8V ~ +5V) for all of 4 ports
- Support Battery Charger (BC1.2) detection
- -40˚C to 85˚C operating temperature
- QFN64 package (RoHS compliant and Pb-free Green Compound)

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REVISION HISTORY

Revision	Description	Date
1.0	- Formal release	2025-5-2

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Product Data Sheet PL2543

1. Product Applications

- Single-chip upgrade solution for Legacy RS232 devices to USB interface
- USB to RS232/RS422/RS485 interface converters/cables/dongles/adapters
- MCU-based devices to USB host interface
- Point-of-Sale (POS) Terminals/Printers/Pole Displays
- USB Barcode/Smart Card Readers
- PC I/O Docking Station/Port Replicators
- Healthcare/Medical USB Interface Data Transfer Cable
- Serial-over-IP Wireless Solution
- Cellular/PDA USB Interface Data Transfer Cable
- GPS/Navigation USB Interface
- Industrial / Instrumentation / Automation Control USB Interface
- USB Modem / Wireless / Zigbee USB Interface
- Set-Top Box (STB) / Home Gateway USB Interface
- Battery Charger Detection for high-current and quick charging of batteries.

2. Royalty-Free Driver Support

- Windows 11, 10, 8, 7 (Microsoft Certified WHQL Drivers)
- Windows Server 2008 R2, 2012, 2016, 2019, 2022, 2025
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2543	64-pin QFN (9x9mm)	PL2543A2FKG7P1	260pcs / tray
		PL2543A2FKG8P1	2000pcs / reel

This packaging is applicable to MSL 3 (Based on IPC/JEDEC J-STD-020) for MPQ (Minimum Package Quantity)

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4. Block Diagram

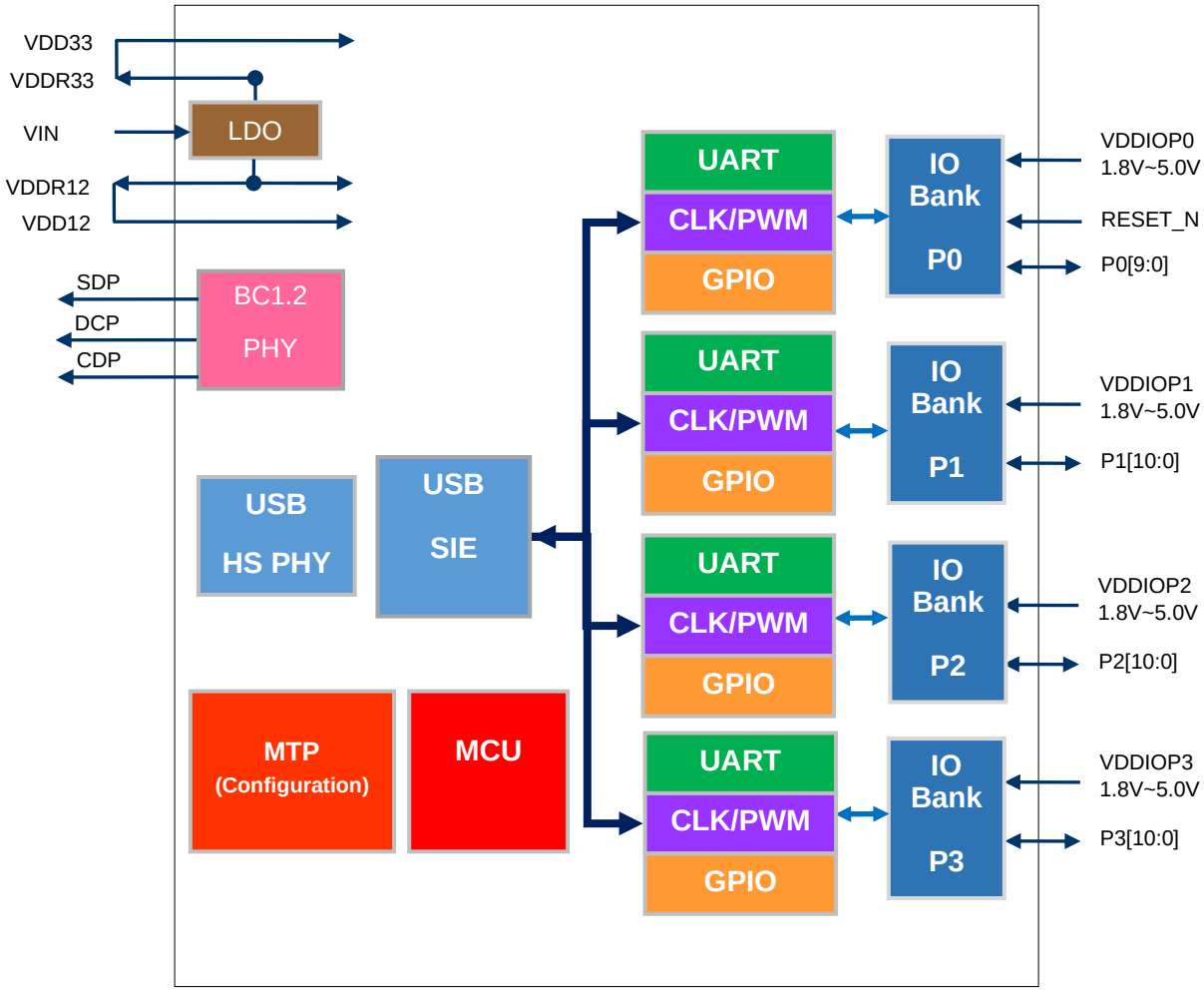

Figure 4-1: PL2543 Block Diagram

5. USB Logo Certification

The PL2543 IC has been certified by the USB-IF organization with TID 6180 to be fully compliant with the USB 2.0 specification.

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6. Overview

The PL2543 is a full-featured single-chip USB CDC to UART bridge controller for connecting 4 COM port full-duplex UART asynchronous serial interface device to any Universal Serial Bus (USB) capable host. The PL2543 provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most operating systems allowing existing serial UART applications based on legacy COM port to easily migrate and be made USB ready.

The PL2543 also integrates an USB 2.0 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and MTPROM.

The PL2543 added several new features and enhancements:

- New USB drivers for different OS platforms with faster performance and advanced features.
- Precise baud rate generator (up to 24Mbps).
- MTPROM can be programmed directly through USB (no high voltage generator required).
- Individual 512bytes FIFO for IN/OUT buffer per port
- Up to 11 configurable GPIO pins.
- Versatile GPIO functions and routing logic (TX/RX LED, VBUS_DET, USB_CFG, CLK_OUT, etc.).
- Independent and wide I/O voltage range (+1.8V ~ +5V) for all of 4 ports.
- Configurable I/O pin output driving strength.
- UART inverted signal configurable option.
- Unique USB Serial Number for each IC.
- Supports Battery Charger (BC1.2) Detection to enable fast charging of batteries.

The PL2543 is available in 64-pin QFN package with Pb-free (RoHS compliant) green package.

7. Pin Assignment & Description

7.1 PL2543 Pin Assignment

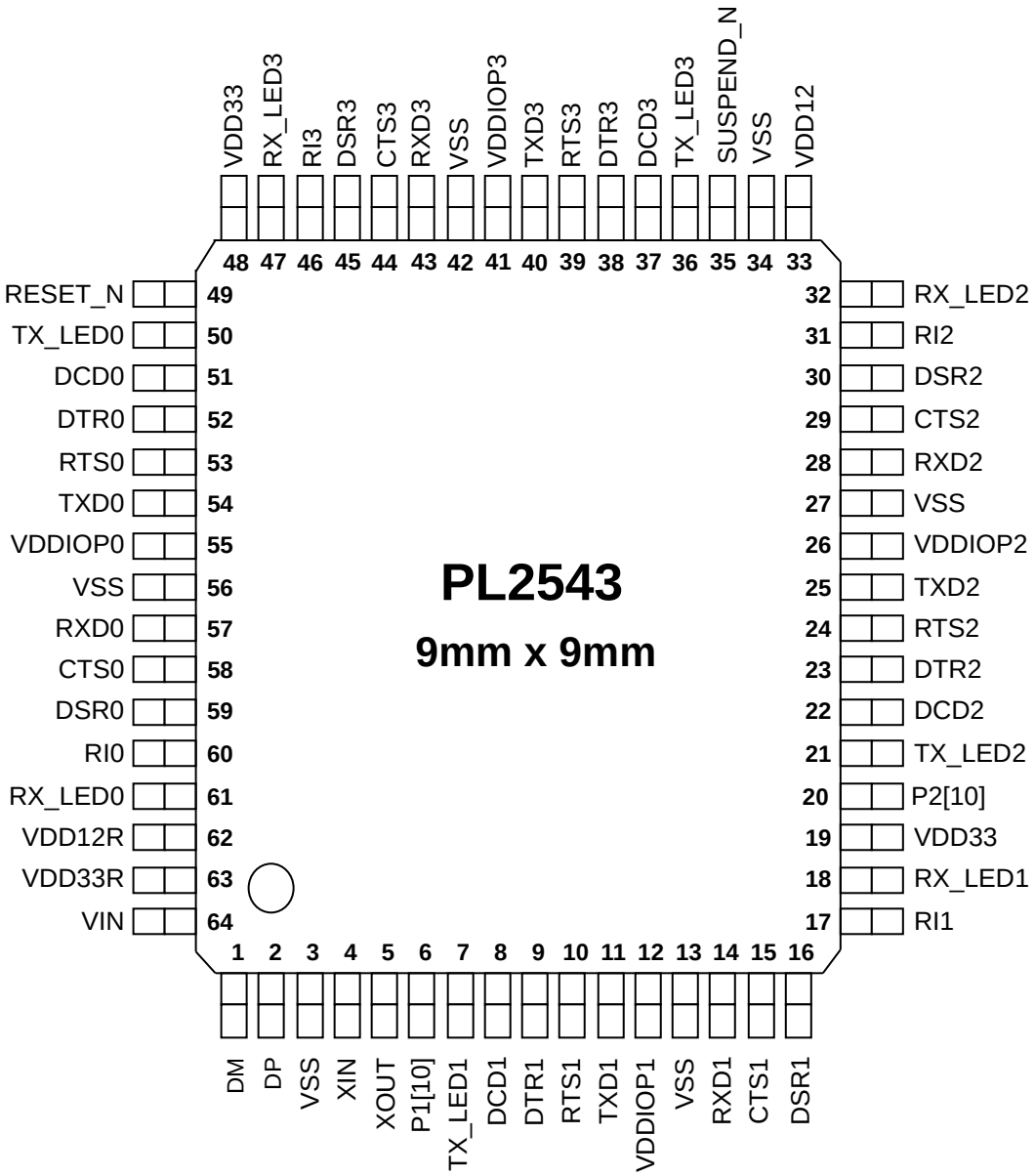


Figure 7-1: PL2543 Pin Diagram

7.2 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	QFN64 Pin No.	Type	Description
DP	2	I/O	USB Port Data Plus (D+) Signal.
DM	1	I/O	USB Port Data Minus (D-) Signal.

Table 7-2: UART (Serial Port) Interface Pins

Pin Name	QFN64 Pin No.	Type	Description
TXD0	54	Output	P0 Serial Port: Transmitted Data Output
DTR0	52	Output	P0 Serial Port: Data Terminal Ready Control Output
RTS0	53	Output	P0 Serial Port: Request To Send Control Output
RXD0	57	Input	P0 Serial Port: Received Data Input
RI0	60	Input	P0 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR0	59	Input	P0 Serial Port: Data Set Ready Control Input
DCD0	51	Input	P0 Serial Port: Data Carrier Detect Control Input
CTS0	58	Input	P0 Serial Port: Clear To Send Control Input
TXD1	11	Output	P1 Serial Port: Transmitted Data Output
DTR1	9	Output	P1 Serial Port: Data Terminal Ready Control Output
RTS1	10	Output	P1 Serial Port: Request To Send Control Output
RXD1	14	Input	P1 Serial Port: Received Data Input
RI1	17	Input	P1 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR1	16	Input	P1 Serial Port: Data Set Ready Control Input
DCD1	8	Input	P1 Serial Port: Data Carrier Detect Control Input
CTS1	15	Input	P1 Serial Port: Clear To Send Control Input
TXD2	25	Output	P2 Serial Port: Transmitted Data Output
DTR2	23	Output	P2 Serial Port: Data Terminal Ready Control Output
RTS2	24	Output	P2 Serial Port: Request To Send Control Output
RXD2	28	Input	P2 Serial Port: Received Data Input
RI2	31	Input	P2 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR2	30	Input	P2 Serial Port: Data Set Ready Control Input
DCD2	22	Input	P2 Serial Port: Data Carrier Detect Control Input
CTS2	29	Input	P2 Serial Port: Clear To Send Control Input
TXD3	40	Output	P3 Serial Port: Transmitted Data Output
DTR3	38	Output	P3 Serial Port: Data Terminal Ready Control Output
RTS3	39	Output	P3 Serial Port: Request To Send Control Output
RXD3	43	Input	P3 Serial Port: Received Data Input
RI3	46	Input	P3 Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR3	45	Input	P3 Serial Port: Data Set Ready Control Input
DCD3	37	Input	P3 Serial Port: Data Carrier Detect Control Input
CTS3	44	Input	P3 Serial Port: Clear To Send Control Input

NOTE: All input pins of UART function are default pull up

Table 7-3: Configurable GPIO Pins –

Pin Name	QFN64 Pin No.	Type	Description
TX_LED0	50	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED0	61	I/O	Configurable GPIO Pin. (see Section 7.2)
TX_LED1	7	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED1	18	I/O	Configurable GPIO Pin. (see Section 7.2)
TX_LED2	21	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED2	32	I/O	Configurable GPIO Pin. (see Section 7.2)
TX_LED3	36	I/O	Configurable GPIO Pin. (see Section 7.2)
RX_LED3	47	I/O	Configurable GPIO Pin. (see Section 7.2)
P1[10]	6	I/O	Configurable GPIO Pin. (see Section 7.2)
P2[10]	20	I/O	Configurable GPIO Pin. (see Section 7.2)
SUSPEND_N	35	O	Active low shutdown control pin during USB suspend.

NOTE: All GPIO pins are default Input mode.

Table 7-4: Power and Ground Pins

Pin Name	QFN64 Pin No.	Type	Description
VDDIOP0	55	Power	+1.8V to +5V P0 I/O signal power input pin. **Note: VDD_IO voltage should not larger than VIN voltage.**
VDDIOP1	12	Power	+1.8V to +5V P1 I/O signal power input pin.
VDDIOP2	26	Power	+1.8V to +5V P2 I/O signal power input pin.
VDDIOP3	41	Power	+1.8V to +5V P3 I/O signal power input pin.
VDD33R	63	Power	+3.3V LDO regulator output.
VDD33	19,48	Power	+3.3V Power input
VDD12R	62	Power	+1.2V LDO regulator output. **Note: Shall not be used for supplying external other circuits.**
VDD12	33	Power	+1.2V Power input
VSS	3, 13, 27, 34,42,56,65(Exposed Pad)	Power	Ground
VIN	64	Power	LDO regulator input. Supply power of +4.0V - +5.25V

Table 7-5: Miscellaneous Pins

Pin Name	QFN64 Pin No.	Type	Description
RESET_N	49	Input	Active low external reset pin is used to reset the PL2543. NOTE: This pin is internally pulled high.
XI	4	Input	12MHz crystal oscillator input.
XOUT	5	Output	12MHz crystal oscillator output.

Pin Type:

- AIO – Analog Bi-directional
- DI – Digital Input
- DIO – Digital Bi-directional
- P – Power / Ground

7.3 GPIO Multi- Function Options

The PL2543 chip (QFN64 package) provides a total of 11 configurable GPIO (General Purpose I/O) pins. The pins are grouped into P0, P1, P2 and P3 set of pins. The table below shows the possible functions that can be configured for each GPIO pin. be configured for each GPIO pin. These special functions can be easily configured in the MTPROM of the PL2543 or to an external I2C EEPROM using the Prolific MTPROM/EEPROM software tool. When these pins are configured as standard GPIO pins, customers can refer to the Prolific GPIO SDK (software development kit) to develop software to control the GPIO pins for desired functions in customer application.

Table 7-6: Configurable GPIO Multi-Function Pins

GPIO	QFN64 Pin No.	Factory Default	Configurable Options (using MTP Tool)			
P0[0]	54	TXD0				
P0[1]	57	RXD0				
P0[2]	53	RTS0				
P0[3]	58	CTS0				
P0[4]	52	DTR0				
P0[5]	59	DSR0	PWMB0			
P0[6]	51	DCD0	PWMA0			
P0[7]	60	RI0 (WAKEUP)				
P0[8]	50	TX_LED0	GPIO	TX_EN0	CLK0	
P0[9]	61	RX_LED0	GPIO	TRX_LED0	CLK0	BC_DET
P0[10]	49	RESET_N				
P1[0]	11	TXD1				
P1[1]	14	RXD1				
P1[2]	10	RTS1				
P1[3]	15	CTS1				
P1[4]	9	DTR1				
P1[5]	16	DSR1	PWMB1			
P1[6]	8	DCD1	PWMA1			
P1[7]	17	RI1(WAKEUP)				
P1[8]	7	TX_LED1	GPIO	TX_EN1	CLK1	
P1[9]	18	RX_LED1	GPIO	TRX_LED1	CLK1	BC_SUSP_N[1]
P1[10]	6	GPIO	VBUS_DET	SLK		
P2[0]	25	TXD2				
P2[1]	28	RXD2				
P2[2]	24	RTS2				
P2[3]	29	CTS2				

P2[4]	23	DTR2				
P2[5]	30	DSR2	PWMB2			
P2[6]	22	DCD2	PWMA2			
P2[7]	31	RI2(WAKEUP)				
P2[8]	21	TX_LED2	GPIO	TX_EN2	CLK2	
P2[9]	32	RX_LED2	GPIO	TRX_LED2	CLK2	USB_CFG_N
P2[10]	20	GPIO	USB_CFG	SDA		
P3[0]	40	TXD3				
P3[1]	43	RXD3				
P3[2]	39	RTS3				
P3[3]	44	CTS3				
P3[4]	38	DTR3				
P3[5]	45	DSR3	PWMB3			
P3[6]	37	DCD3	PWMA3			
P3[7]	46	RI3(WAKEUP)				
P3[8]	36	TX_LED3	GPIO	TX_EN3	CLK3	
P3[9]	47	RX_LED3	GPIO	TRX_LED3	CLK3	SUSPEND
P3[10]	35	SUSPEND_N	GPIO			

Note :

1. BC_SUSP_N = (SUSPEND_N | BC_DET)
2. There are 7 different special functions (BC_SUSP_N, BC_DET, SUSPEND, SUSPEND_N, VBUS_DET, USB_CFG, USB_CFG_N). Positive and negative functions are treated as different functions. For example, SUSPEND and SUSPEND_N are different functions.
3. Though multiple location candidates, each special function can only be assigned to one location (pin).

Table 7-7: GPIO Multi-Function Option Descriptions

GPIO Function	QFN64 GPIO Pins	Type	Description
TX_LED [0:3]	P0[8] (Pin 50) P1[8] (Pin 7) P2[8] (Pin 21) P3[8] (Pin 36)	Output	Serial Port: TXD [0:3] Access LED during transmitting data.
RX_LED [0:3]	P0[9] (Pin61) P1[9] (Pin18) P2[9] (Pin32) P3[9] (Pin47)	Output	Serial Port: RXD [0:3] Access LED during receiving data.
TRX_LED [0:3]	P0[9] (Pin61) P1[9] (Pin18) P2[9] (Pin32)	Output	Serial Port: TXD[0:3]/RXD [0:3] Access LED during transmitting or receiving data.

	P3[9] (Pin47)		
VBUS_DET	P1[10](Pin6)	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level. There must be only one pin configured as VBUS_DET pin. Refer above note for this special function.
USB_CFG_N	P2[9] (Pin32)	Output	This active low signal is used to indicate USB device has been attached and configured by USB host. So system may detect this pin to enable function after USB configuration. Refer to above note for this special function.
USB_CFG	P2[10] (Pin20)	Output	This active high signal is used to indicate USB device has been attached and configured by USB host. So system may detect this pin to enable function after USB configuration. Refer to above note for this special function.
TX_EN [0:3]	P0[8] (Pin 50) P1[8] (Pin 7) P2[8] (Pin 21) P3[8] (Pin 36)	Output	Transmit Data Enable Pin can be used to enable RS485/RS422 transceiver when data is being transmitted.
SUSPEND_N	P3[10] (Pin35)	Output	Active low shutdown control pin during USB suspend. This pin is used to indicate chip entering suspend state when USB bus in idle state. Refer to above note for this special function.
SUSPEND	P3[9] (Pin47)	Output	Active high shutdown control pin during USB suspend. This pin is used to indicate chip entering suspend state when USB bus in idle state. Refer to above note for this special function.
WAKEUP	P0[7] (Pin 60) P1[7] (Pin 17) P2[7] (Pin 31) P3[7] (Pin 46)	Input	The remote wakeup function is to wake up chip from suspended state when this pin toggle in suspend state. There must be only one pin configured as WAKEUP pin. The factory default is RI[0:3] .
BC_DET	P0[9] (Pin61)	Output	Battery Charge Detect pin. This active high pin indicates BC 1.2 DCP/CDP is detected.
BC_SUSP_N	P1[9] (Pin18)	Output	This pin has same function as SUSPEND pin only if BC function is enabled and detected.
CLK [0:3]	P0[8] (Pin 50) P0[9] (Pin61) P1[8] (Pin 7) P1[9] (Pin18) P2[8] (Pin 21) P2[9] (Pin32)	Output	Each channel has an independent clock output for external application. CLK[n] output pin can be configured to Pn[8] or Pn[9]. The n is channel number. This pin can generate clock output up to 12MHz. Clock rates can be configured in

	P3[8] (Pin 36) P3[9] (Pin47)		MTPROM/EEPROM or customized driver.
PWMA [0:3]	P0[6] (Pin51) P1[6] (Pin8) P2[6] (Pin22) P3[6] (Pin37)	Output	There are 2 independent PWMA and PWMB modules in the chip. Its max. frequency is about 7.6MHz. Users can refer to the programming guide in PL2543 SDK for details about how to enable PWM function and set its frequency and duty cycle.
PWMB [0:3]	P0[5] (Pin59) P1[5] (Pin16) P2[5] (Pin30) P3[5] (Pin45)	Output	There are 2 independent PWMA and PWMB modules in the chip. Its max. frequency is about 7.6MHz. Users can refer to the programming guide in PL2543 SDK for details about how to enable PWM function and set its frequency and duty cycle.
SDA	P2[10](Pin20)	Input/ Output	External I2C EEPROM interface serial data signal.
SCL	P1[10](Pin6)	Input/ Output	External I2C EEPROM interface serial clock signal.

8. Functional description

8.1 BC 1.2 Detection

This function is used to detect VBUS power supply capability of USB host port and provides charging control to battery charging IC. This function is enabled in MTPROM by setting GPIO pin to BC_DET option. This pin will indicate if BC 1.2 DCP/CDP is detected when device is attached to the USB port. The external battery charging IC uses the USB_CFG and SUSP_N signal pins to control its charging current support or the BC_DET signal pin to enable fast charging current mode.

8.2 USB 2.0 HS Transceiver

The USB Transceiver provides the USB high/full-speed electrical signal requirements and USB physical interface (DP/DM). This block includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal. And the R_{REF} (resistor for reference power) also is included to save BOM cost.

8.3 LDO Regulator

This block is the 5V to 3.3V and 1.2V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components

8.4 USB HS/FS SIE

The USB High/Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB HS/FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB HS/FS transceiver to parallel data for internal circuit. This block includes 15 IN/OUT endpoints. So there are sufficient multi interfaces supported by PL2543. Using these endpoints, it can implement multi functions in a single chip.

8.5 MCU

There is a MCU inside to handle USB standard requests and vendor requests. Many different configurations can be applied if different settings is configured in MTP. The MCU will depend on the value in MTP to do related setting for different implementation.

8.6 Internal MTPROM

The MTPROM (Multi-Time Programming Memory) is used as MCU firmware and chip function settings, GPIO pin function setting and USB descriptor related data. There is 768 bytes user programming area available for customization settings. This user programming area can be easily programmed by the Prolific MTPROM software through USB port without any additional voltage converter requirement.

8.7 UART Control

There are 4 UART control modules handle the data transfer according to RS232 format and interface. Each module has full flow control, including hardware RTS/CTS, DTR/DSR and software flow control. So it can support RS232, PS485, modem etc. The IO voltage level supports wild range from 1.8 to 5.0 V. Baud rate also supports wild range from 5Hz to 24MHz and these baud rate setting is easily set by popular terminal tool through USB command.

8.8 IO Functions

The IO Functions block implements generic GPIO function and many configurable I/O functions such as TX access LED and RX access LED features, clock output features with PWM, and others.

8.9 IO Routing Logic

The PL2543 has many versatile I/O functions. Each GPIO pin includes multiple functions that can be configured in the MTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

8.10 I^2C EEPROM Controller

The I2C EEPROM Controller provides an optional alternative solution to the MTPROM that allows an external I2C EEPROM to be attached through GPIO pins 6 and 20 (P1[10]/ P2[10]) for the SLK and SDA interface. Using the PL2543 MTPROM/EEPROM Writer program, customer can also write the chip function settings, GPIO pin function settings, and USB descriptor related data to external I2C EEPROM. The advantage of using an external EEPROM is that it can be written several times. The Prolific MTPROM/EEPROM software works by plugging the device through USB port without any additional voltage converter requirement.

9. Design Application Example

This section illustrates conceptual design application examples using the PL2543.

9.1 3.3V Self Powered Design

Because minimum input voltage of the internal 5V to 3.3V LDO regulator is 4.0V for the requirement of 3.3V output voltage, the internal LDO can’t be used for the application that VIN pin is under 4V. For the application of 3.3V operating power, users should keep the VIN pin NC(floating) and can use external 3.3V power supply for all of 3.3V power pins of PL2543 which are VDD33R and VDD33 . Please refer to PL2543 reference schematic for the application of 3.3V operating power.

10. AC & DC Characteristics

10.1 Absolute Maximum Ratings

Table 10-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{VIN}	Power supply of VIN	-0.3 to 5.5	V
V_{DD12}	Power supply of VDD12	-0.3 to 1.3	V
V_{DD33}	Power supply of VDD33	-0.3 to 3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	+1.8 to V_{VIN}[1]	V
$V_{VDDIOP3}$	Power supply of VDDIOP3	+1.8 to V_{VIN}[1]	V
V_{INIOP0}	Input voltage of IO of P0	-0.3 to V_{VIN}[1]	V
V_{INIOP1}	Input voltage of IO of P1	-0.3 to V_{VIN}[1]	V
V_{INIOP2}	Input voltage of IO of P2	-0.3 to V_{VIN}[1]	V
V_{INIOP3}	Input voltage of IO of P3	-0.3 to V_{VIN}[1]	V
T_{OP}	Operation temperature	-40 to 85	°C
T_{STG}	Storage temperature	-40 to 150	°C

1: shall not be higher than V_{VIN}

10.2 Operating Current

Table 10-2: Operating Current Parameters

Symbol	Parameter	Min	Typ	Max	Units
I_{VIN}	Current consumption of power supply. Testing condition → 1. bus power mode : power supply by USB VBUS 2. 4 ports operate concurrently without LED/transceiver @ 115200 baud rate.		40		mA
I_{SUS}	Suspend current		900		uA

10.3 Recommended Operating Conditions

Table 10-3: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{VIN}	Power supply of VIN	4.0[2]		5.25	V
V_{DD12}	Power supply of VDD12	1.1	1.2	1.3	V
V_{DD33}	Power supply of VDD33	3.135	3.3	3.6	V
$V_{VDDIOP0}$	Power supply of VDDIOP0	1.8		V_{VIN}[1]	V
$V_{VDDIOP1}$	Power supply of VDDIOP1	1.8		V_{VIN}[1]	V
$V_{VDDIOP2}$	Power supply of VDDIOP2	1.8		V_{VIN}[1]	V
$V_{VDDIOP3}$	Power supply of VDDIOP3	1.8		V_{VIN}[1]	V
V_{INIOP0}	Input voltage of IO of P0	0		V_{VIN}[1]	V
V_{INIOP1}	Input voltage of IO of P1	0		V_{VIN}[1]	V
V_{INIOP2}	Input voltage of IO of P2	0		V_{VIN}[1]	V
V_{INIOP3}	Input voltage of IO of P3	0		V_{VIN}[1]	V

1: shall not be higher than V_{VIN}

2: For using the internal 3.3V power from the internal 5-3.3V LDO

10.4 IO Characteristics

Table 10-4: IO Characteristics at VDDIO=1.8V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=1.8V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.1			V
VIL		Input low voltage				0.8	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
I_{OH}	DRV=1	Driving high current	VIO >= 0.9*VDDIO			1.8	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			2.1	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			2.3	mA
I_{OL}	DRV=1	Driving low current	VIO <= 0.1*VDDIO			4	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			6	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			8	mA
T_{RISE}	DRV=1	Rise time	20pF loading, 10% to 90%		28		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		25		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		23		ns
T_{FALL}	DRV=1	Fall time	20pF loading, 90% to 10%		0.7		ns
	DRV=2	Fall time	20pF loading, 90% to 10%		0.6		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		0.5		ns

FBAUD	DRV=1	UART baud rate		5		12M	bps
	DRV=2	UART baud rate		5		12M	bps
	DRV=3	UART baud rate		5		12M	bps
RPULLUP		Pull-up resistance			75.6K		Ohm
RPULLDOWN		Pull-down resistance			72K		Ohm
ILEAKHI		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		23		uA
ILEAKLO		Input low leakage	VIO = 0V Pull-up/pull-down disabled		23		uA

Table 10-5: IO Characteristics at VDDIO=3.3V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=3.3V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.4			V
VIL		Input low voltage				1.3	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
IOH	DRV=1	Driving high current	VIO >= 0.9*VDDIO			11	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			17	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			22	mA
IOL	DRV=1	Driving low current	VIO <= 0.1*VDDIO			12	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			18	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			24	mA
TRISE	DRV=1	Rise time	10pF loading, 10% to 90%		4		ns
	DRV=2	Rise time	10pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	10pF loading, 10% to 90%		2		ns
TFALL	DRV=1	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=2	Fall time	10pF loading, 90% to 10%		1		ns
	DRV=3	Fall time	10pF loading, 90% to 10%		1		ns
FBAUD	DRV=1	UART baud rate		5		24M	bps
	DRV=2	UART baud rate		5		24M	bps
	DRV=3	UART baud rate		5		24M	bps
RPULLUP		Pull-up resistance			75.6K		Ohm
RPULLDOWN		Pull-down resistance			72K		Ohm

I_{LEAKHI}		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		43		uA
I_{LEAKLO}		Input low leakage	VIO = 0V Pull-up/pull-down disabled		43		uA

Table 10-6: IO Characteristics at VDDIO=5.0V

VIN=5.0V, VDD33=3.3V, VDD12=1.2V, **VDDIO=5.0V**, T=25 °C

Symbol		Parameter	Test Condition	Min	Typ	Max	Units
VIH		Input high voltage		1.5			V
VIL		Input low voltage				1.3	V
VOH		Output high voltage	IIO <= IOH	0.9*VDDIO			V
VOL		Output low voltage	IIO <= IOL			0.1*VDDIO	V
I_{OH}	DRV=1	Driving high current	VIO >= 0.9*VDDIO			20	mA
	DRV=2	Driving high current	VIO >= 0.9*VDDIO			28	mA
	DRV=3	Driving high current	VIO >= 0.9*VDDIO			38	mA
I_{OL}	DRV=1	Driving low current	VIO <= 0.1*VDDIO			20	mA
	DRV=2	Driving low current	VIO <= 0.1*VDDIO			28	mA
	DRV=3	Driving low current	VIO <= 0.1*VDDIO			36	mA
T_{RISE}	DRV=1	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=2	Rise time	20pF loading, 10% to 90%		2		ns
	DRV=3	Rise time	20pF loading, 10% to 90%		1.5		ns
T_{FALL}	DRV=1	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=2	Fall time	20pF loading, 90% to 10%		1.5		ns
	DRV=3	Fall time	20pF loading, 90% to 10%		1.5		ns
F_{BAUD}	DRV=1	UART baud rate		5		24M	bps
	DRV=2	UART baud rate		5		24M	bps
	DRV=3	UART baud rate		5		24M	bps
R_{PULLUP}		Pull-up resistance			75.6K		Ohm
$R_{PULLDOWN}$		Pull-down resistance			72K		Ohm
I_{LEAKHI}		Input high leakage	VIO = VDDIO Pull-up/pull-down disabled		65		uA
I_{LEAKLO}		Input low leakage	VIO = 0V Pull-up/pull-down disabled		65		uA

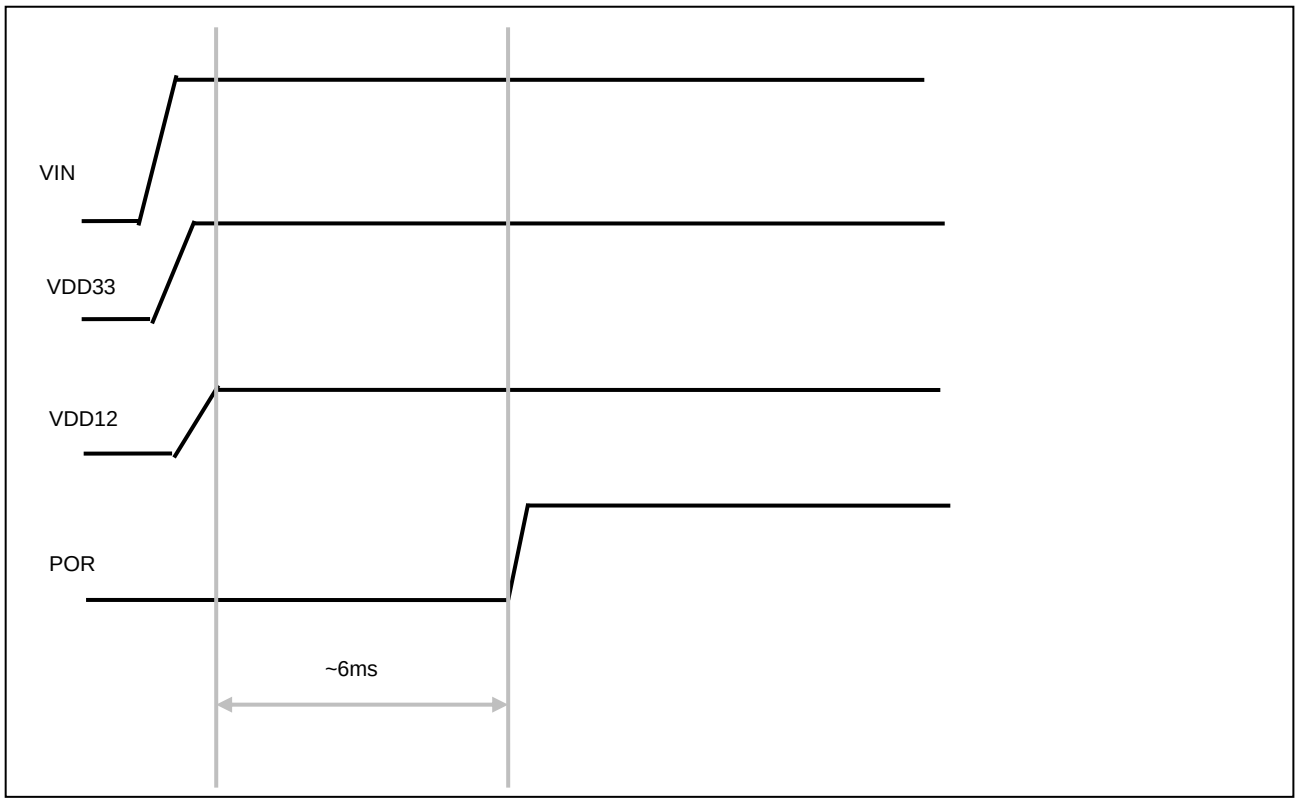
10.5 Timing parameters

Table 10-7: Timing parameters

Symbol	Parameter	Min	Typ	Max	Units
T_{POR}			6		ms

Chip Reset Control

The PL2543 has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help system designs to make sure of chip operation start time.



10.6 Temperature Characteristics

Table 10-8: Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

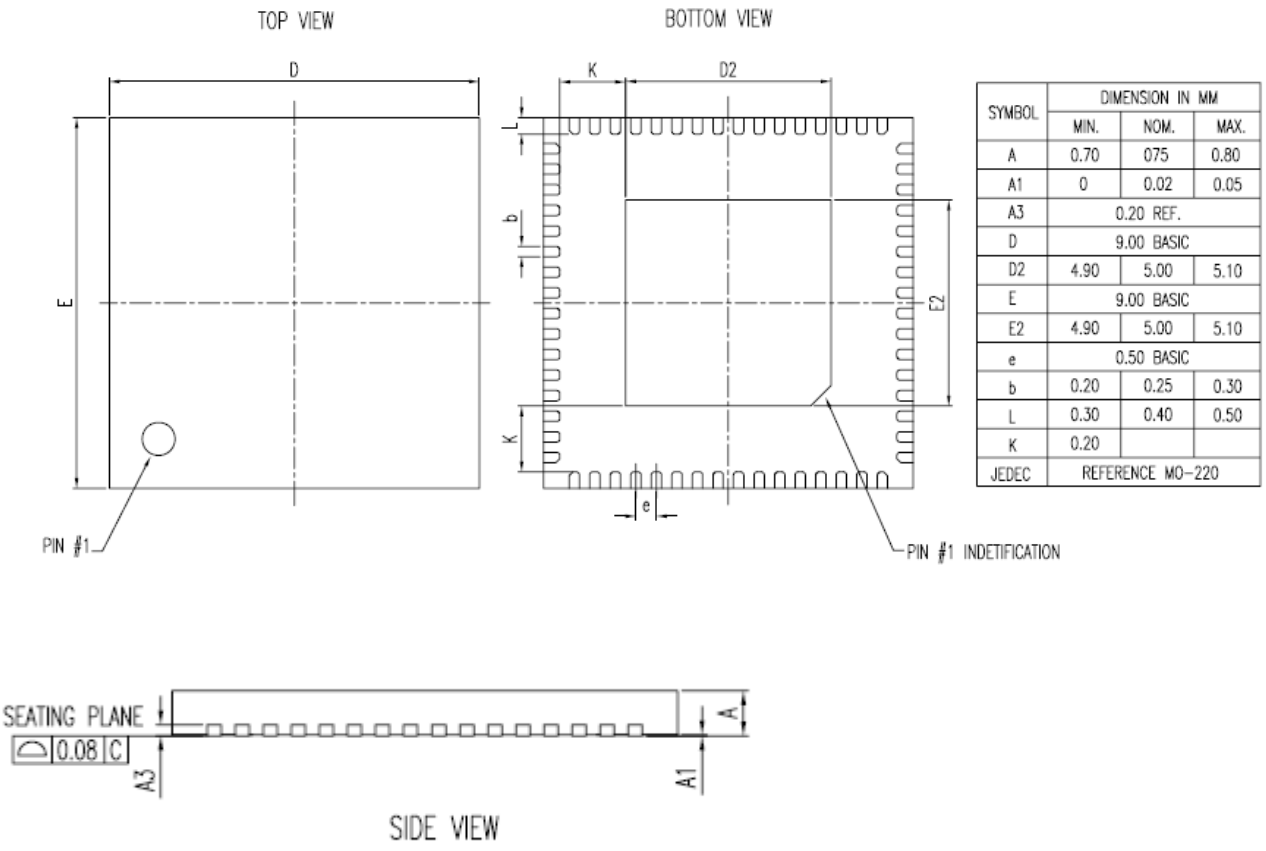
10.7 Baud Rate Characteristics

Table 10-9: Baud Rate Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Baud rate @ VDD_IO = 5V	--	5	--	24M	bps
Baud rate @ VDD_IO = 3.3V	--	5	--	24M	bps
Baud rate @ VDD_IO = 1.8V	--	5	--	12M	bps

11. IC outline information

11.1 Outline Diagram



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	075	0.80
A1	0	0.02	0.05
A3	0.20 REF.		
D	9.00 BASIC		
D2	4.90	5.00	5.10
E	9.00 BASIC		
E2	4.90	5.00	5.10
e	0.50 BASIC		
b	0.20	0.25	0.30
L	0.30	0.40	0.50
K	0.20		
JEDEC	REFERENCE MO-220		

Figure 11-1: PL2543 Outline Diagram (QFN64 9x9mm)

11.2 IC Marking information

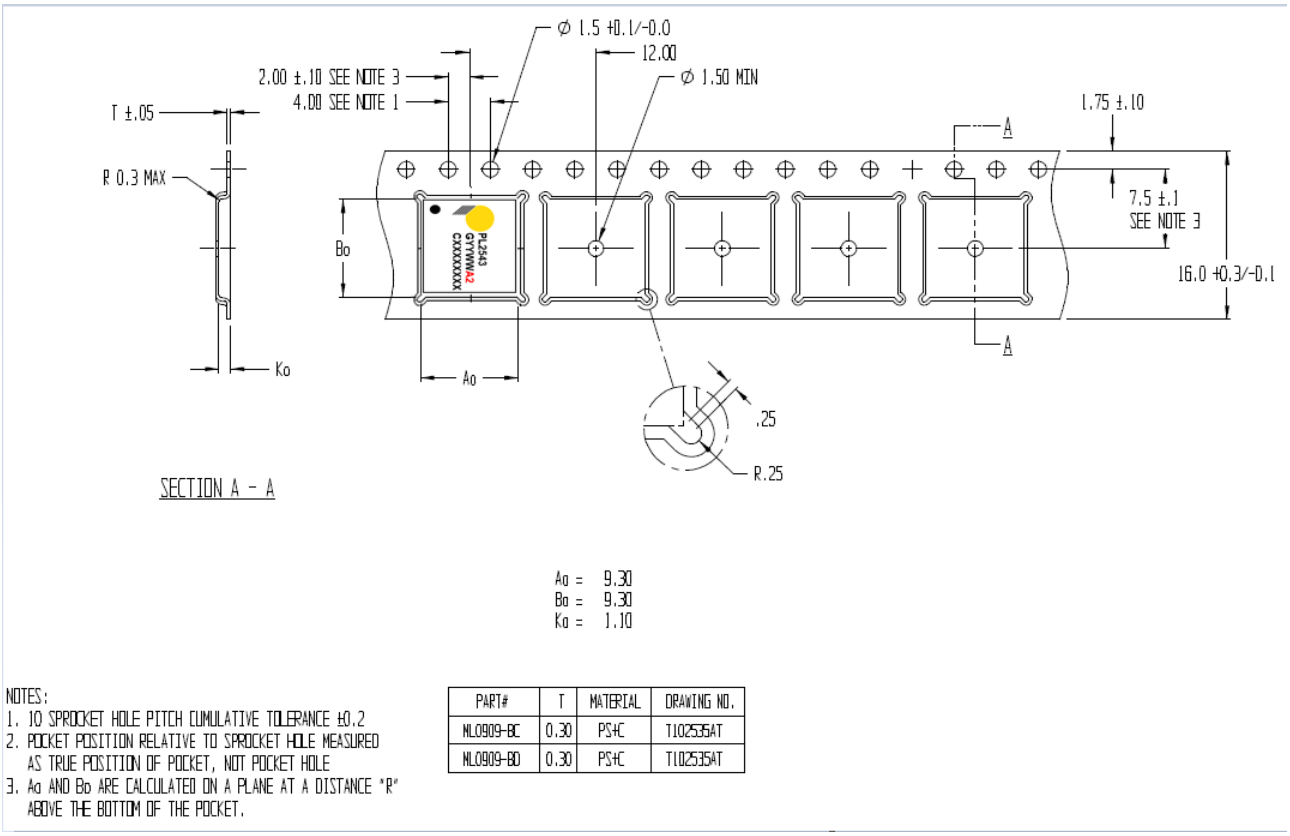
Table 11-1: IC Marking Information

Line	Marking	Description
First Line	PL2543	Chip Product Name
Second Line (GYYWWXX)	G	Green packing material
	YY	Last two digits of the manufacturing year
	WW	Week number of the manufacturing year
	XX	Chip Version
Third Line	XXXXXXXXX	9-digit manufacturing LOT code

Example: "*G2316A1*" – means Green packing + Year 2023 + Week no. 16 + A1 chip version.

12. Package material information

12.1 Carrier Tape(QFN64)



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

PART#	T	MATERIAL	DRAWING NO.
NL0909-BC	0.30	PS+C	T102535AT
NL0909-BD	0.30	PS+C	T102535AT

Figure 12-1: QFN64 Carrier Tape

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