PL23D3
USB HID to SPI Bridge Controller with GPIO

USB Interface

- Fully Compliant with USB 2.0 specification (Full-Speed Mode).
- UHCI/OHCI (USB 1.1), EHCI (USB 2.0), xHCI (USB 3.1) Host Controller Compatible.
- USB Human Interface Device (HID) class:
  - No driver installation needed for Windows, Mac, Linux, and Android.
  - Provides HID-to-SPI SDK (DLL libraries) for application development.
- Highly integrated USB 1.1 FS Transceiver. Integrated termination resistors and pull-up resistor to reduce PCB external components.
- Supports 256-byte OTPROM (One-Time Programmable ROM) programming by software tool via USB interface for USB device descriptors and GPIO configuration.
- Each IC has unique ID (for Serial Number).
- Supports USB power configuration (bus-powered, self-powered)

SPI Serial Interface

- Supports SPI Master mode.
- Supports clock rate up to 4.8MHz.
- 1024-byte bi-directional data buffers (768-byte receive/256-byte transmit).
- Supports two Chip Select lines.
- Support clock polarity options(Inverse or not).
- Supports remote wakeup pin signal.

Battery Charger Detection

- Supports Battery Charger (BC1.2) detection to enable fast charging of batteries.

GPIO Interface

- Total 9 General Purpose I/O (GPIO) pins.
- Versatile GPIO functions and routing logic provides easy to use multi-I/O functions:
  - Configurable I/O pin output driving strength.
  - Clock Output to external MCU (CLK_OUT).
  - VBUS input detectionto to trigger PL23D3 attachment to USB host controllers (VBUS_DET).
  - USB configured state indication function (USB_CFG).
  - Suspend state indication function (SUSP_N).

➢ GPIOs can be controlled by custom software applications via USB interface.

Miscellaneous

- Integrated self-generated precise clock generator (No external crystal required).
- Integrated Power-on-Reset (POR) circuit.
- Wide input operating voltage 2.8 - 5.5V
- Integrated 5V to 3.3V LDO that can support 80mA for external components
- Low operating power and USB suspend current.
- Wide I/O voltage range (1.8V/2.5V/3.3V/5V).
- -40^{o}C to 85^{o}C Operating Temperature.
- Available in 16-pin QFN package (RoHS compliant and Pb-free Green Compound).

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Website：http://www.prolific.com.tw/

REVISION HISTORY

Revision	Description	Date
1.03	➢ To add the pin description of e-Pad in Table 7-5: Miscellaneous Pins	2023/11/24
1.0.2	➢ To change SSOP16 in Table 7-3 and 7-6 as QFN16	2022/11/8
1.0.1	➢ To change the quantity of MPQ in ordering info.from 5K to 4K ➢ To remove and add the supported OS of SDK -removed OS: Win Server 2003, 2008 -added OS: Win Server 2019	2020/9/9
1.0.0	➢ Formal release	2020/3/11

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Product Data Sheet PL23D3

1. Product Applications

- USB to SPI Master Controller
- HID Device Controller
- Sensor/Touch Controller
- Memory: Flash and EEPROM
- Battery Charger Detection for high-current and quick charging of batteries.

2. HID to SPI API Library Support

Human Interface Device (HID) class is natively supported in almost all operating systems. No custom driver is required to be installed. Prolific provides SDK and Dynamic-Link Library (DLL) for customers to develop their application software. Refer to the PL23D3 HID to SPI SDK documentation on how to control the PL23D3 using the DLL.

- Windows 10, 8, 7, Vista, XP
- Windows Server 2008R2, 2012, 2016, 2019
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL23D3	16-pin QFN	PL23D3G4FGG8P1	4000pcs / reel

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4. Block Diagram

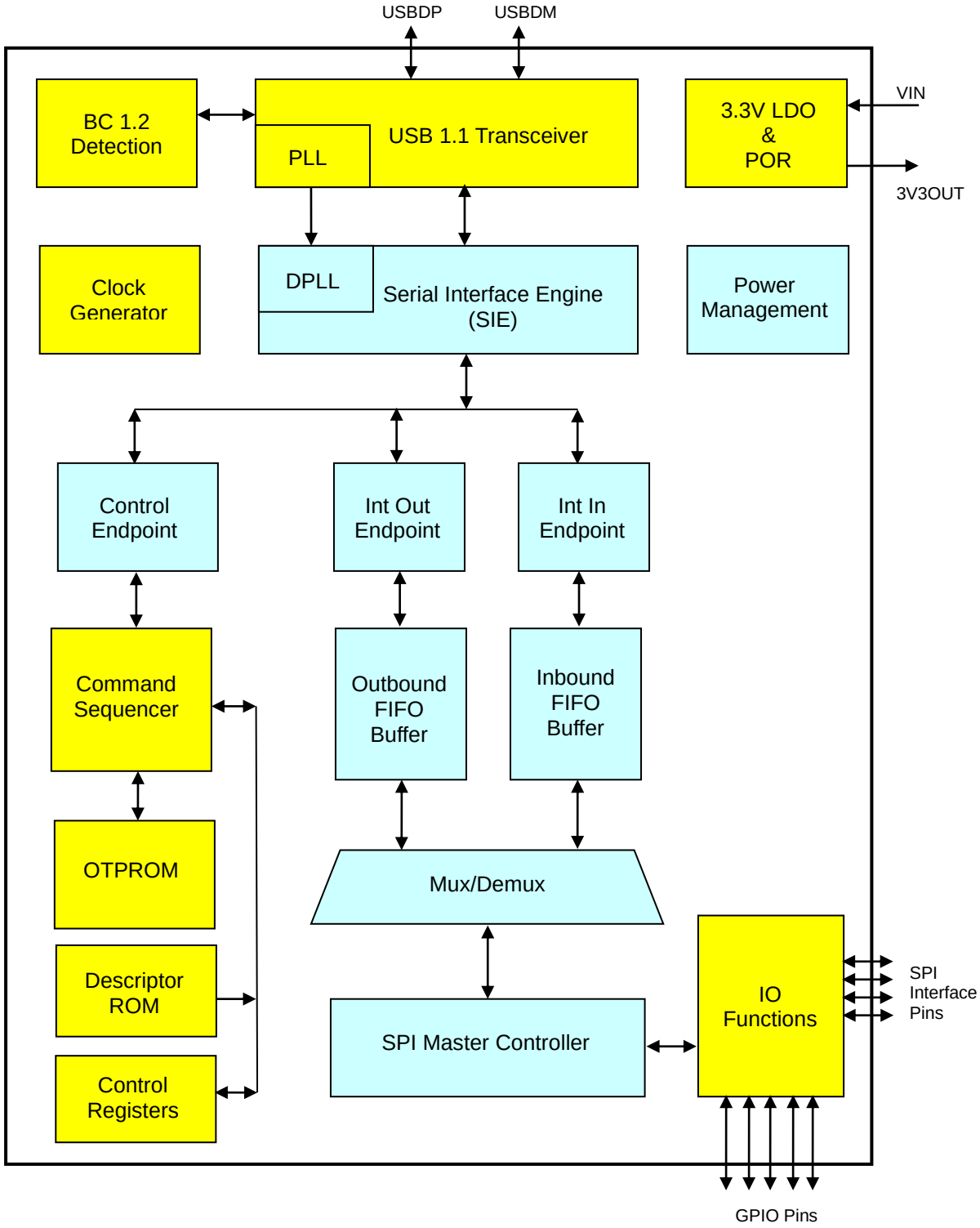

Figure 4-1 PL23D3 Block Diagram

5. USB Logo Certification

(TBA)

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6. Overview

The PL23D3 is a high performance single-chip USB HID to SPI bridge controller for connecting various SPI interface devices to any Universal Serial Bus (USB) capable host. The PL23D3 implements the standard USB Human Interface Device (HID) device class which is natively supported in most operating systems; so the PL23D3 does not need any custom driver installation. The operating system or USB host communicates with the PL23D3 through HID to SPI application software developed based on Windows/Mac/Linux DLL libraries provided by Prolific.

The PL23D3 integrates an internal precise clock generator (no external crystal required), USB 1.1 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and One-Time Programming ROM (OTPROM). The OTPROM allows vendors to customize some USB descriptors and configurations like USB Vendor ID (VID), Product ID (PID), Manufacturer and Product strings, USB Serial Number, power configuration as well as GPIO configurations.

The PL23D3 is designed to support a wide-range of SPI domain including portable, embedded, industrial, consumer devices. With very small power consumption in either operating or suspend mode, the PL23D3 is perfect for self-powered operation and can reserve power for the attached SPI devices. Flexible signal voltage option allows the PL23D3 to connect directly to SPI devices with 5V~1.8V signals..
The PL23D3 is available in 16-pin QFN footprint RoHS compliant and Pb-free green compound package.

7. Pin Diagram and Description

7.1 QFN16 Pin Diagram

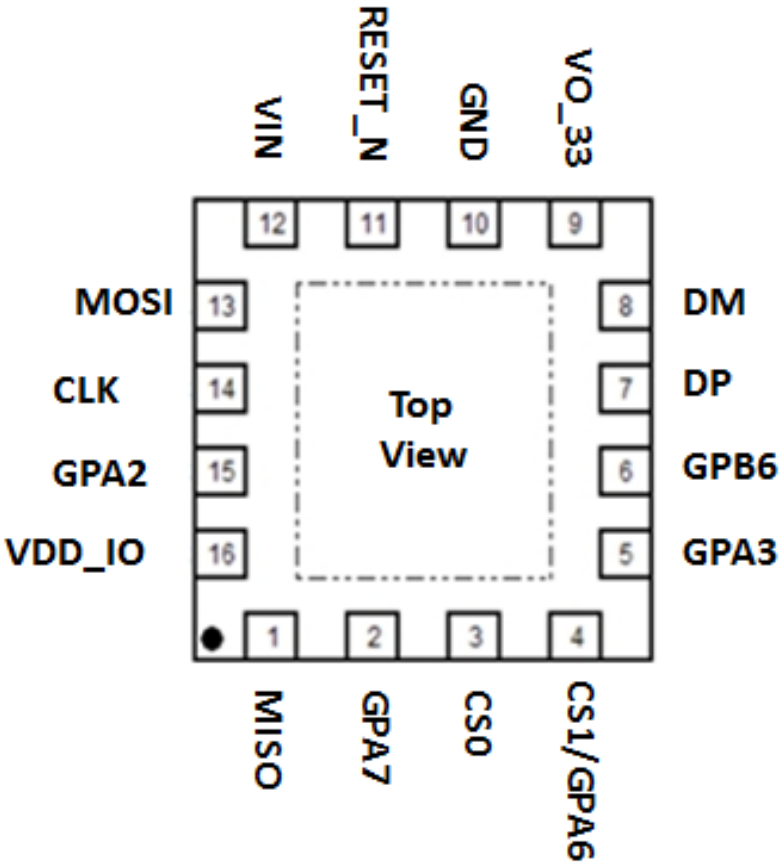

Figure 7-1 PL23D3 Pin Diagram (QFN16)

7.2 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	QFN16 Pin No.	Type	Description
DP	7	I/O	USB Port Data Plus (D+) Signal
DM	8	I/O	USB Port Data Minus (D-) Signal

Table 7-2: SPI Bus Interface Pins

Pin Name	QFN16 Pin No.	Type	Description
MOSI	13	Output	Master Output Slave Input
MISO	1	Input	Master Input Slave Output
CLK	14	Output	SPI Master Serial Clock Output
CS0	3	Output	SPI Slave Select 0
CS1	4	Output	SPI Slave Select 1

Table 7-3: Configurable GPIO Pins

Pin Name	QFN16 Pin No.	Type	Description
GPA0	13	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is MOSI**
GPA1	1	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is MISO**
GPA2	15	I/O	Configurable GPIO Pin. (see Section 7.3)
GPA3	5	I/O	Configurable GPIO Pin. (see Section 7.3)
GPA4	14	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is SPI_CLK (SPI Serial Clock).**
GPA5	3	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is SPI_CS0 (SPI Slave Select 0).**
GPA6	4	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is SPI_CS1 (SPI Slave Select 1).**
GPA7	2	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is WAKEUP input pin.**
GPB6	6	I/O	Configurable GPIO Pin. (see Section 7.3) **Factory default is SUSP_N output pin.**

Table 7-4: Power and Ground Pins

Pin Name	QFN16 Pin No.	Type	Description
VDD_IO	16	Power	+1.8V to +5V I/O signal power input pin. VDD_IO supply voltage should not be larger than VIN voltage.
VO_33	9	Power	+3.3V output power from integrated LDO regulator. For self-powered design, supply +3.3V to this pin.
GND	10	Power	Ground
VIN	12	Power	USB port VBUS input power supply. For self-powered design, supply +3.3V to this pin.

Table 7-5: Miscellaneous Pins

Pin Name	QFN16 Pin No.	Type	Description
RESET_N	11	Input	Active low Reset pin. Can be used by external device to reset the PL23D3. This pin has internal pull-up to VDD_IO.
Exposed Pad	17	NC	No internal connection. Leave floating.

7.3 GPIO Multi-Function Options

The PL23D3 chip provides a total of 9 configurable GPIO (General Purpose I/O) pins. The pins are grouped into 8 GPA and 1 GPB set of pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the OTPROM of the PL23D3. When these pins are configured as standard GPIO pins, customers can refer to the PL23D3 HID to SPI SDK to develop software on how to control the GPIO pins for customer application desired functions.

Table 7-6: Configurable GPIO Multi-Function Pins

GPIO	QFN16 Pin No.	Factory Default	Configurable Options (using OTPROM Tool)		
GPA0	13	**MOSI**			
GPA1	1	**MISO**			
GPA2	15	**GPIO**	CLK_OUT	SUSP_N	USB_CFG
GPA3	5	**GPIO**	WAKEUP	VBUS_DET	BC_DET
GPA4	14	**SPI_CLK**			
GPA5	3	**SPI_CS0**	BC_SUSP_N		
GPA6	4	**SPI_CS1**			
GPA7	2	**WAKEUP**			
GPB6	6	**SUSP_N**	USB_CFG	WAKEUP	CLK_OUT

Table 7-7: GPIO Multi-Function Option Descriptions

GPIO Function	QFN16 GPIO Pins	Type	Description
VBUS_DET	GPA3	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level.
USB_CFG	GPA2 GPB6	Output	When device is attached to USB port and configured by USB host, this USB_CFG pin will output to high level. This pin can be used to enable system function after USB is configured.
SUSP_N	GPA2 GPB6	Output	Active low Shutdown control pin. This pin has two options to choose. One is to indicate chip suspend state by USB bus state. The other option (factory default) is to indicate chip un-configured state and chip suspend state. These two options can be configured in OTPROM.
WAKEUP	GPA3 GPA7 GPB6	Input	The remote wakeup function is to wake up chip from suspended state when this pin toggle from high to low in suspend state. There must be only one pin configured as WAKEUP pin. The factory default is GPA7 pin.
BC_DET	GPA3	Output	Battery Charge Detect pin. This active high pin indicates BC 1.2 DCP/CDP is detected.

BC_SUSP_N	GPA5	Output	This pin has same function as SUSP_N except this pin will be forced inactive in chip suspend state when BC 1.2 DCP/CDP is detected.
CLK_OUT	GPA2 GPB6	Output	This pin can generate clock output up to 12MHz. Clock rates can be configured in OTPROM. There must be only one pin configured as CLK_OUT pin.

8. Functional Description

This section details the functional block diagram description of the PL23D3. The PL23D3 is a HID to SPI bridge controller that implements standard USB HID device class. The USB HID device class is natively supported by most operating systems so custom driver is not required to be installed. USB HID devices exchange data between the host via HID reports using software developed application. Prolific provides DLL (dynamic-link libraries) with easy API for PL23D3 HID to SPI application development.

8.1 BC 1.2 Detection

This function is used to detect VBUS power supply capability of USB host port and provides charging control to battery charging IC. This function is enabled in OTPROM by setting GPIO pin to BC_DET option. This pin will indicate if BC 1.2 DCP/CDP is detected when device is attached to the USB port. The external battery charging IC uses the USB_CFG and SUSP_N signal pins to control its charging current support or the BC_DET signal pin to enable fast charging current mode.

8.2 USB 1.1 FS Transceiver

The USB Transceiver provides the USB full-speed electrical signal requirements and USB physical interface (DP/DM). This block also includes one precise internal oscillator for PLL. The PLL provides the clock to other logic functions. This block also includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal.

8.3 LDO Regulator

This block is the 5V to 3.3V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components.

8.4 Clock Generator

The clock generator module generates the 48MHz and 12MHz reference clock signals for internal chip logic. The internal clocks will be stopped while in suspend state.

8.5 USB FS SIE

The USB Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB FS transceiver to parallel data for internal circuit. This block supports USB packet decoding and encoding. It also generates and check packet CRC, bit stuffing, SYNC and EOP frame signal. The DPLL module will

use the internal 48MHz clock to synchronize external DP/DM transitions to generate 12MHz clock for USB interface related circuit.

8.6 Power Management

This module will monitor the USB attachment and DP/DM signals state to create reset state, running state, suspend state, wakeup state, etc.

8.7 Control Endpoint

The Control Endpoint module handles control endpoint packet transfer protocols such as SETUP packet, DATA packet and return status packet.

8.8 Interrupt Out Endpoint

The Interrupt Out Endpoint module handles interrupt-out endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers USB host interrupt-out data to chip outbound FIFO.

8.9 Interrupt In Endpoint

The Interrupt In Endpoint module handles interrupt-in endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers data inside the chip inbound FIFO to USB host through interurpt-in DATA packet.

8.10 Command Sequencer

This module handles the USB standard requests and vendor requests. It dispatches control signals to relative peripheral modules and gather information from peripheral modules. When it received USB standard request commands, it may check ROM data or data latched from OTP and return them to USB host. When vendor requests are received, it dispatches to peripherals to set or get something.

8.11 Outbound FIFO

This buffer receives data from Interrupt Out Endpoint and provides data to SPI controller modules. It handles read and write pointers and calculate full and empty conditions.

8.12 Inbound FIFO

This buffer receives data from SPI controller modules and provides data to Interrupt In Endpoint. It handles read and write pointers and calculate full and empty conditions.

8.13 Internal OTPROM

The OTPROM (One-Time Programming Read-Only Memory) is used to store chip function settings, GPIO pin function setting and USB descriptor related data. A one-time programming user area of the memory is available to allow customization of settings. The user area of the PL23D3 OTPROM can now be easily programmed using the PL23D3 OTPROM software tool through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM configuration settings.

8.14 Mux/Demux

This module is designed to pass data between FIFO and peripheral module.

8.15 Descriptor ROM

This block contains the USB descriptor data for returning to USB host.

8.16 SPI Master Control

The SPI Master control module follow SPI specification to access SPI slave devices. The SPI master provides the MOSI (Master Out Slave In) or SPI_OUT pin as master data output, MISO (Master In Slave Out) or SPI_IN pin as data input, SPI_CLK pin as master clock output, and two Slave Select pins output to select SPI device. The SPI Master Control module supports single data bit transfer. This module uses 48MHz as clock source to generate SPI signals. It supports maximum 4.8MHz SPI clock speed. The clock signal polarity and clock sample phase can be changed according to SPI specification.

8.17 Control Registers

The Control Registers module contains the chip control registers read and set, and initially loads from OTPROM. USB host will use USB vendor command to read and write control registers to set chip function.

8.18 IO Functions

The IO Functions block implements generic GPIO function and many configurable I/O functions such as clock output features, and others (see Section 7.3). The PL23D3 has many versatile I/O functions. Each GPIO pin is provided with multiple functions that can be configured in the OTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

9. Chip Function Configuration

The default configuration descriptors are stored in the chip internal memory which will be loaded during power-on reset or USB bus reset whenever OTPROM is empty. Several of the USB and configuration descriptors could be modified and programmed one-time into the chip's OTPROM using the PL23D3 OTPROM Writer utility program via the USB port. These descriptors include Vendor ID, Product ID, Serial Number, Product String, GPIO configurations, and other configuration descriptors.

9.1 USB Data Configuration

Table 9-1 USB Descriptor Configuration

Descriptors	Default Value	Description
OTPROM Space	1	This field indicates the space left for the OTPROM that can be written (1 or 0). The OTPROM can only be written once and cannot be erased. If value is 0, it means OTPROM has already been written once.
Vendor ID (VID)	067B (hex)	USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF. Refer to this website for applying VID: http://www.usb.org/developers/vendor/
Product ID (PID)	2362 (hex)	USB Product ID assigned by Manufacturer.
Release No. (BCD)	0100 (hex)	This field reports the release number of the USB device chip. This item is not allowed to be modified.
Device Power Mode	Bus Powered (100mA)	This field sets the USB device if bus-powered or self-powered device.
Max Power	100mA	This field sets the USB device maximum power that can be drawn by the device from the USB host. Enter the value here if it is not 100mA or 500mA. Expressed in 2 mA units (i.e., 50 = 100 mA).
USB Selective Suspend	Enable	This field enables/disables the USB Selective Suspend function. When enabled, Windows OS will suspend the device when idle for few seconds (COM port not open).
Manufacturer String	Prolific Technology Inc.	This field contains the product manufacturer string.
Product String	USB to SPI Controller	This field contains the product string.

Serial Number	Enable Unique Serial Number ID	• Disable Serial Number – this option will disable the Serial Number. Operating System will assign a random serial number for the device.
		• Enable Unique Serial Number ID – this default option enables the unique serial number pre-programmed inside the chip.
		• Custom Serial Number – this option allows the customer to set own product serial numbering:
		  ○ Auto SN: allows to add prefix while the numbers auto increment after each write.
		  ○ Fixed SN: this will write the same number.

NOTE: The total string length for the manufacturer + product + serial number string is up to 90 characters.

9.2 GPIO (GPA) Configuration

Also refer to Section 7.3 for the complete GPIO Multi-Function options description.

Table 9-2 GPIO (GPA Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPA0	SPI_OUT	Output	This field also allows setting the pin as a standard GPIO. • SPI_OUT (default) • GPIO (General Purpose I/O)
GPA1	SPI_IN	Input	This field also allows setting the pin as a standard GPIO. • SPI_IN (default) • GPIO (General Purpose I/O)
GPA2	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • CLK_OUT (also refer to MISC folder) • SUSP_N (also refer to MISC folder) • USB_CFG • GPIO (General Purpose I/O)
GPA3	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • WAKEUP • VBUS_DET (also refer to MISC folder) • BC_DET • GPIO (General Purpose I/O)
GPA4	SPI_CLK	Output	This field allows setting the pin as a standard GPIO or any of the following function: • SPI_CLK (default) • GPIO (General Purpose I/O)
GPA5	SPI_CS0	Output	This field allows setting the pin as a standard GPIO or any of the following function: • SPI_CS0 (default) • BC_SUSP_N • GPIO (General Purpose I/O)
GPA6	SPI_CS1	Output	This field allows setting the pin as a standard GPIO or any of the following function: • SPI_CS1 (default) • GPIO (General Purpose I/O)
GPA7	Wakeup	Input	This field allows setting the pin as a standard GPIO. • Wakeup (default) • GPIO (General Purpose I/O)

Enable Open-Drain	Disabled	This field sets the selected I/O pin to open-drain output mode.
Enable-Pull Up	Disabled	This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to VDD_IO. When enabling pull-up for input pins, the input signal voltage should not be higher than the VDD_IO voltage.**
Inverse Polarity	Disabled	This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA	This field sets the output driving strength of the selected I/O pin. (4mA up to 8mA @ VDDIO3.3V)

9.3 GPIO (GPB) Configuration

Also refer to Section 7.3 for the complete GPIO Multi-Function options description.

Table 9-3 GPIO (GPB Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPB6	SUSP_N	Output	This field allows setting the pin as a standard GPIO or any of the following function: • SUSP_N (default) • GPIO (General Purpose I/O) • USB_CFG • WAKEUP • CLK_OUT (also refer to MISC folder)
Enable Open-Drain	Disabled		This field sets the selected I/O pin to open-drain output mode.
Enable-Pull Up	Disabled		This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to VDD_IO. When enabling pull-up for input pins, the input signal voltage should not be higher than the VDD_IO voltage.**
Inverse Polarity	Disabled		This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA		This field sets the output driving strength of the selected I/O pin. (4mA up to 8mA @ VDDIO3.3V)

10. Design Application Examples

This section illustrates conceptual design application examples using the PL23D3.

10.1 USB Bus Powered Design

The PL23D3 has a built-in 3.3V regulator. USB device power (pin VIN) can be supplied directly from USB VBUS pin. The capacitor behind the USB connector on VBUS is a defined requirement of USB specification. If the regulator output VO_33 needs to be maintained at 3.3V, VIN should be larger than 3.6V.
This built-in 3.3V regulator can supply additional 80mA for external components .

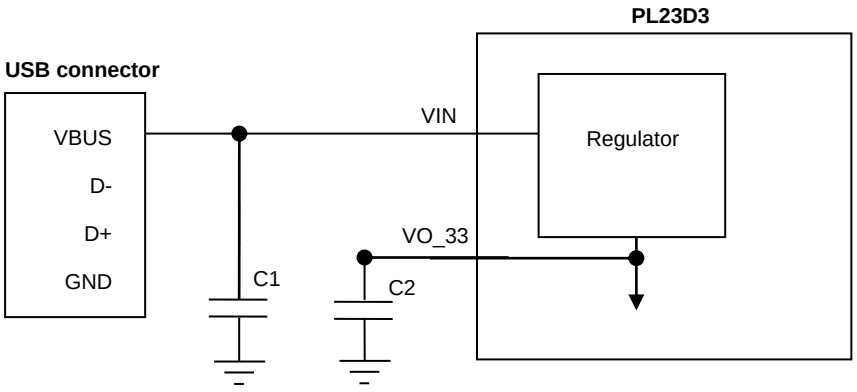

Figure 10-1 USB Bus Powered Design Example

10.2 Self Powered Design

The PL23D3 can also use external power supply. There are two possible ways to use external power source. The first is to use system power source to connect to VIN, and the chip's internal 3.3V regulator will generate the 3.3V power output VO_33 for chip operations and external components. Below Figure 10-2a shows this case. The second is to disable the internal regulator where the system should provide the same 3.3V voltage to VIN and VO_33. Under this condition, the chip will use this external 3.3V power as operating power source. See Figure 10-2b.

For USB self-powered design, it is also recommended to enable the VBUS_DET GPIO input pin function because the PL23D3 DP pin will be pulled up after power on even if USB is not attached yet. USB specification states that a DP pull-up means to attach USB. If the VBUS_DET pin function is turned on and connected to VBUS pin, the chip will only pull-up the DP pin to USB bus when VBUS_DET is active.

To use self-powered design, USB power mode descriptor in the OTPROM of the PL23D3 chip should also be programmed to self-powered mode to match this kind of configuration. USB hosts can read the USB descriptor of the device to know if it is a self-powered device.

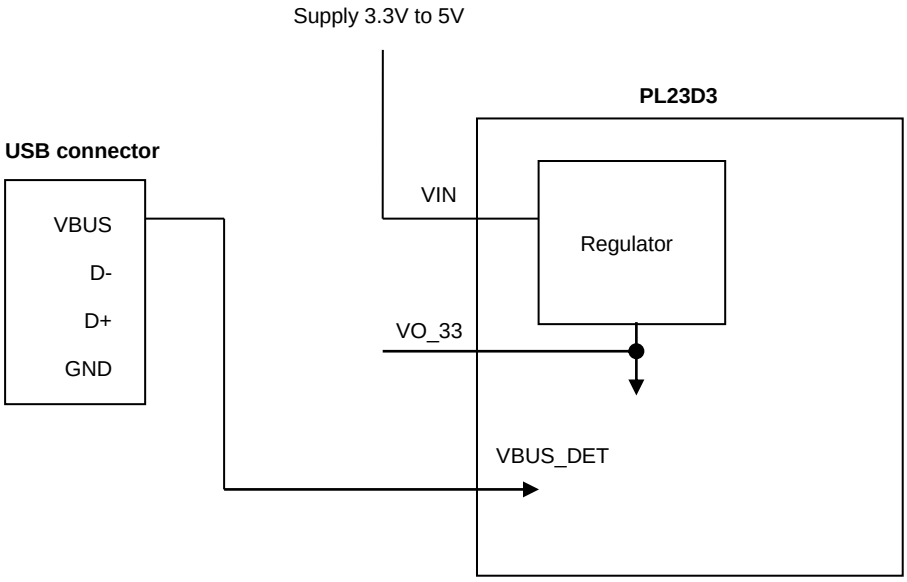

Figure 10-2a USB Self Powered Design Example 1

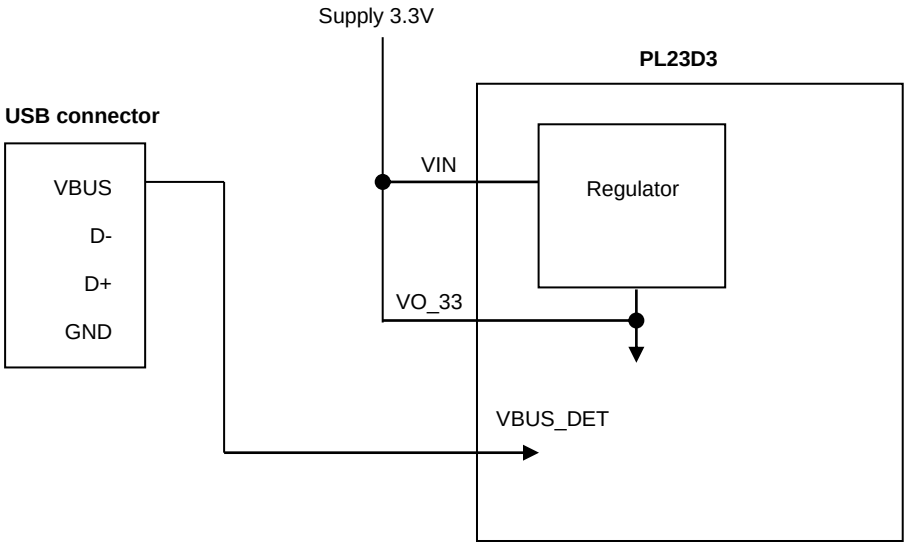

Figure 10-2b USB Self Powered Design Example 2

10.3 Chip Reset Control

The PL23D3 has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help make sure the start time of chip operation.

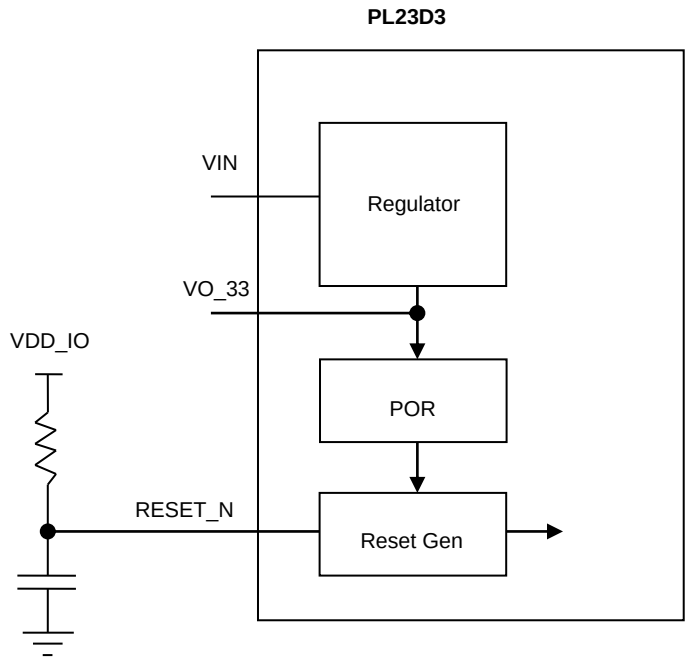

Figure 10-3a Chip Reset Control Application

The power ramp-up time shall keep below than 1ms as shown in diagram below.

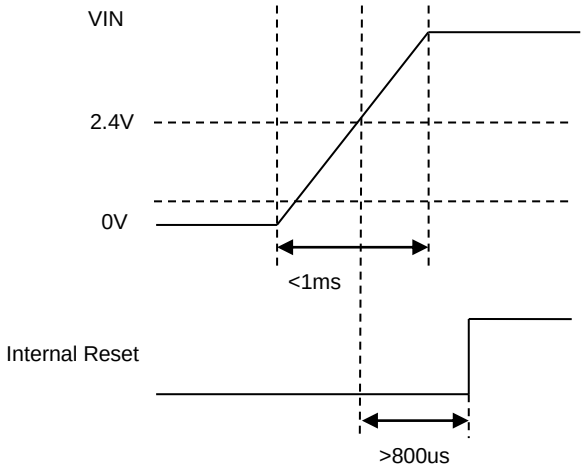

Figure 10-3b Chip Power Reset Timing Diagram

10.4 I/O Power Supply to PL23D3

The PL23D3 supports a wide range of I/O voltage. The simple way to supply IO voltage is to directly connect VDD_IO to VO_33 pin to provide 3.3V I/O voltage. Add capacitor to VDD_IO can help to reduce power noise. Please refer to schematic for the detailed capacitor value.

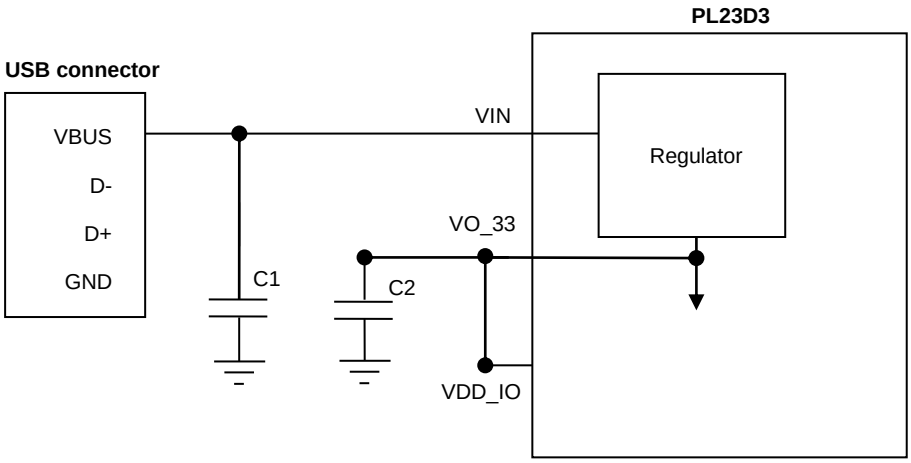

Figure 10-4a IO Power Supply

VDD_IO can also be supplied from other power source to provide different I/O voltage. All of the PL23D3 I/O pins, including SPI signals, use the same VDD_IO voltage. The I/O pins does not support mixed I/O voltages. Unless open-drain option is enabled, the I/O connection between two chips shall use the same VDD_IO voltage. PL23D3 I/O pin also supports 5V tolerance which allows 5V input signal level in different VDD_IO voltage.

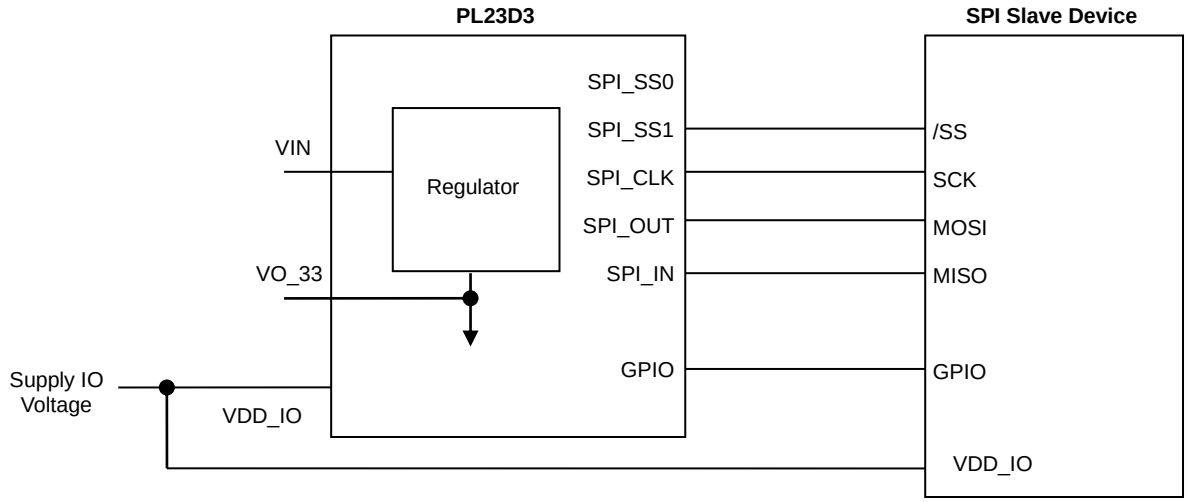

Figure 10-4b VDD_IO Voltage Supply

10.5 Battery Charging Support

The PL23D3 supports USB battery charging specification (BC1.2) wherein battery charging controller can use signals from PL23D3 to control the charging current. An example of charging control concept is shown in below diagram.

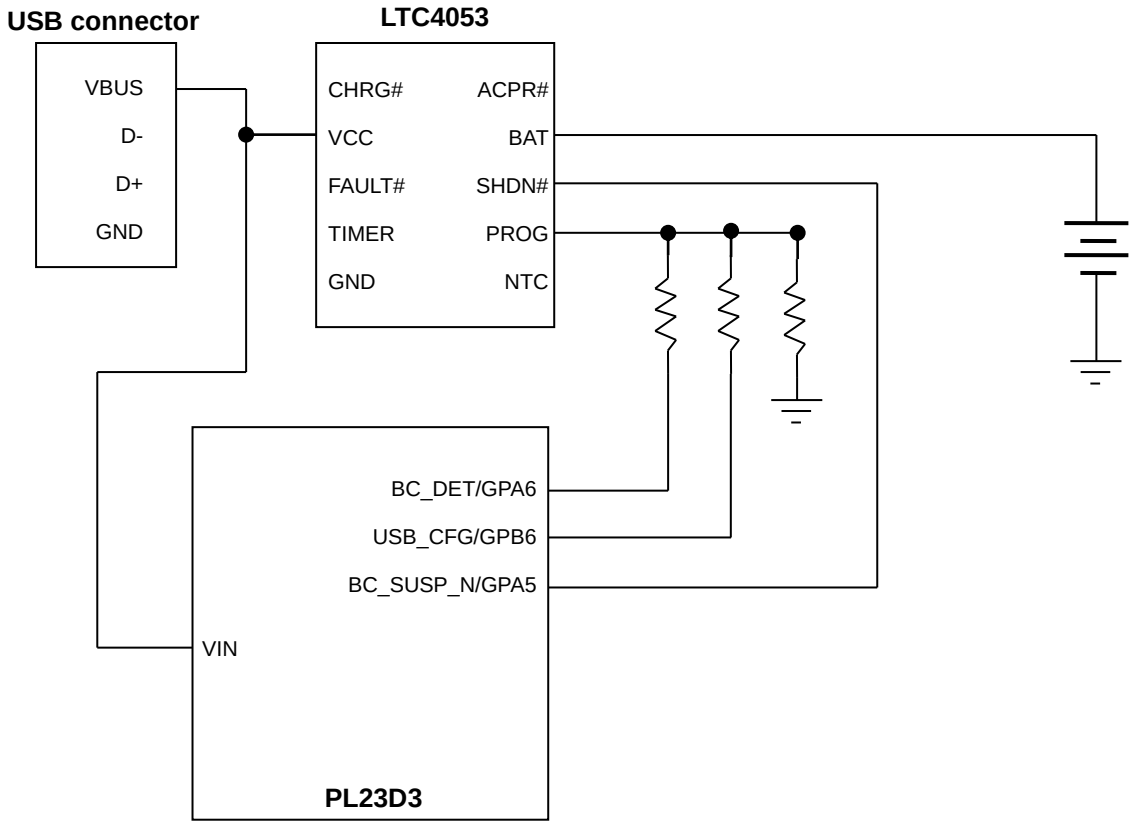

Figure 10-5a Battery Charging Design Example #1

This concept diagram uses the GPA6 GPIO pin configured as BC_DET (battery charge detect pin) signal and this pin need to set to inverse polarity and open-drain mode. GPB6 GPIO pin is configured as USB_CFG and is also set to inverse polarity and open-drain mode. GPA5 GPIO pin is configured as BC_SUSP_N function and connected to shutdown signal of charging controller. All above signals can achieve charging conditions as below table.

Charging Condition	Charging Current (max)	BC_SUSP_N	USB_CFG	BC_DET
Suspend	2.5mA	0	x	x
Un-configured	100mA	1	1	1
Operation	500mA	1	0	1
Fast Charging	1500mA	1	1	0

Below is another example of charging controller support concept.

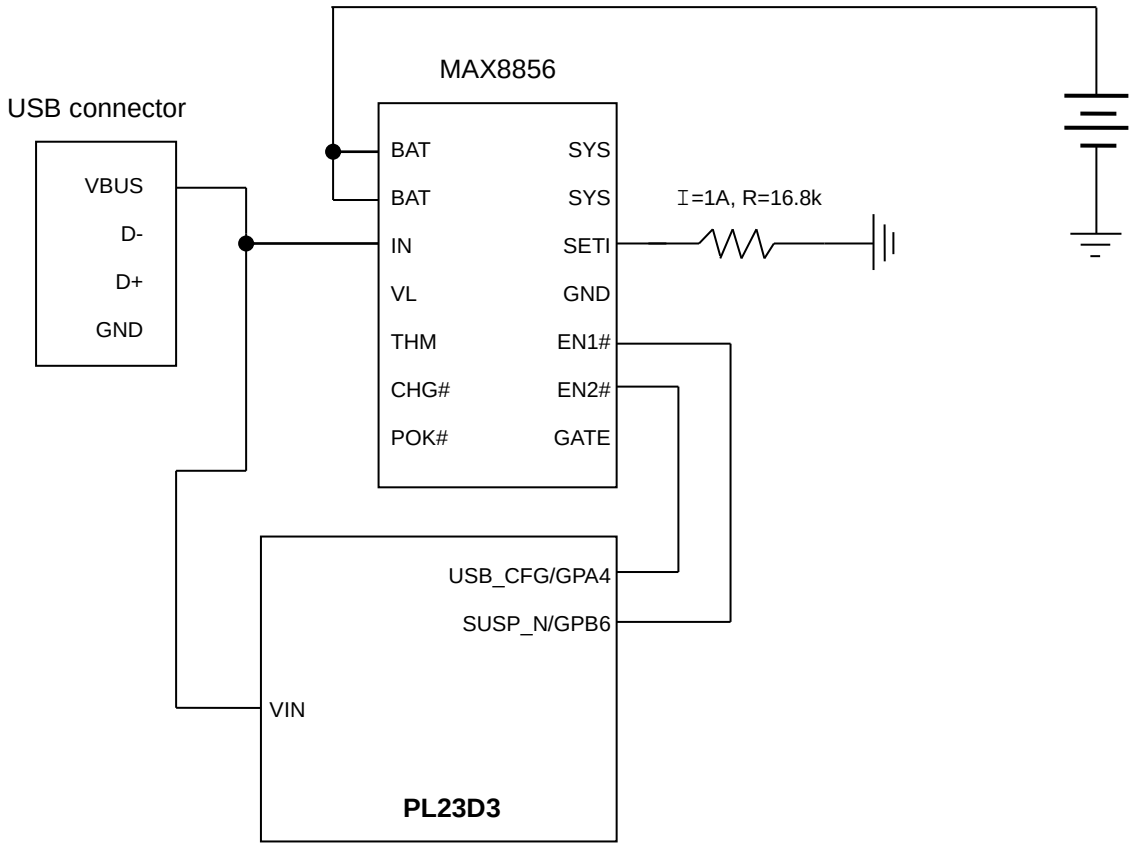

Figure 10-5b Battery Charging Design Example #2

The above concept diagram uses GPA4 pin as USB_CFG and set to normal polarity and push-pull I/O mode as default. GPB6 pin is configured as SUSP_N and set to inverse polarity and push-pull IO mode. The SUSP_N option is also set active during USB bus suspend state only, and not when USB is not configured. This concept diagram can achieve charging conditions as below table.

Charging Condition	Charging Current (max)	SUSP_N	USB_CFG
Suspend	2.5mA	1	1
Un-configured	100mA	0	0
Operation	500mA	0	1
Fast Charging	1000mA	1	0

11. DC & Temperature Characteristics

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage – VIN	-0.3 to 6.0 V
Input Voltage of VDD_IO	-0.3 to VIN+0.3 V
Input Voltage I/O with 5V Tolerance I/O	-0.3 to 6.0 V
Storage Temperature	-40 to 150 °C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

11.2 DC Characteristics

11.2.1 Operating Voltage and Suspend Current

Table 11-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	VIN	2.8	5	5.5	V
Power Supply for I/O Pins	VDD_IO	1.7	3.3	VIN+0.3	V
Output Voltage of Regulator	VO_33	2.97	3.3	3.63	V
Operating Current(1) (Power Consumption)	I_{DD}	-	9.5	15	mA
Suspend Current	I_{SUS}	-	250	450	μA

Note: (1) – No device connected.

11.2.2 I/O Pins

Table 11-2b I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (CMOS)					
Low	V_{IL}	--	--	0.4	V
High	V_{IH}	0.7* VDD_IO	--	--	V
Output Voltage					
Low	V_{OL}	--	--	0.4	V
High	V_{OH}	0.7*VDD_IO	--	--	V

11.3 Temperature Characteristics

Table 11-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

Outline Diagram

12.1 QFN16 Package

SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20 REF.		
D	3.00 BASIC		
D2	1.50	1.65	1.80
E	3.00 BASIC		
E2	1.50	1.65	1.80
e	0.50 BASIC		
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20		
θ	0°		14°
JEDEC	MO-220 (Variation VEED-4)		

Table 12-1 QFN16 Package Dimension

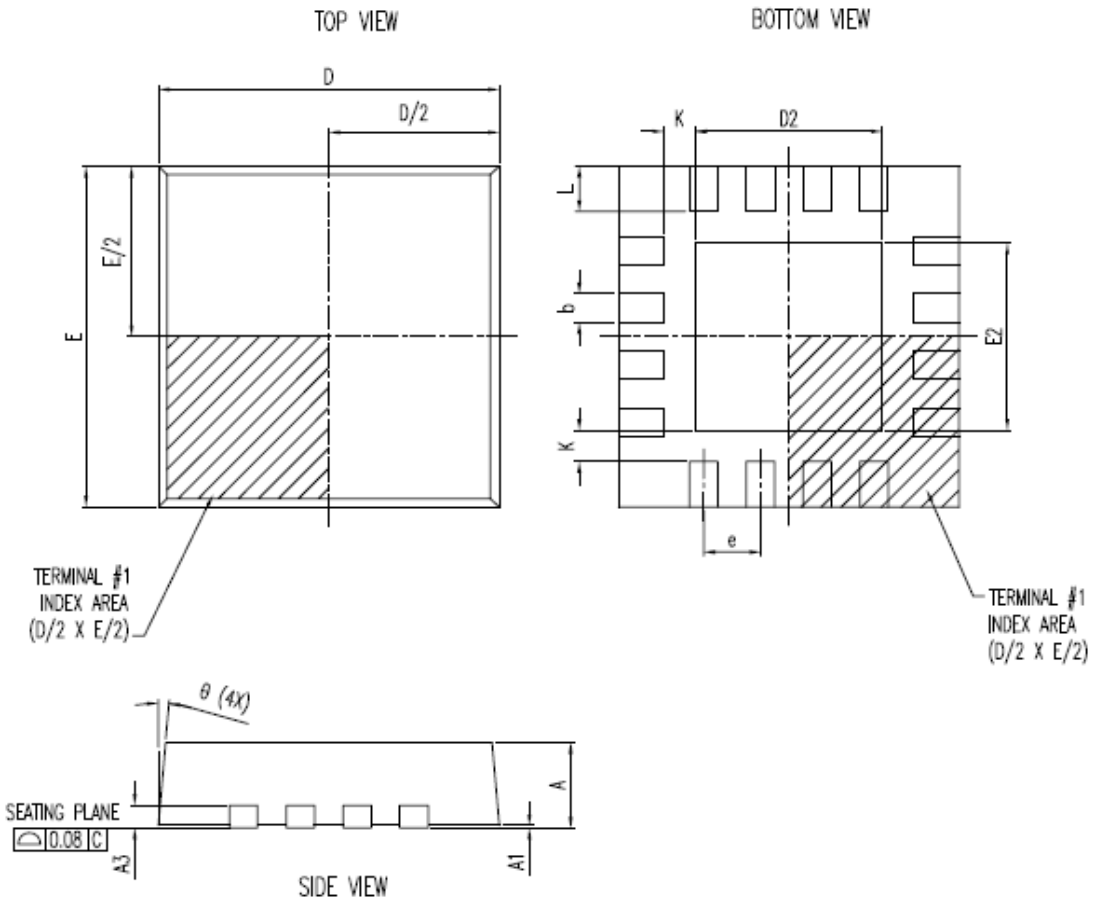

Figure 12-1 PL23D3 Outline Diagram (QFN16)

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