PL2303G series

USB1.1 to UART IC

PCB Layout Guidelines

Document number：AN-23181201

Revision：1.1

Release Date：April 10, 2020

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Overview/概述

The guidelines provide the recommended consideration on PCB layout.
此份指南提供了 PCB 佈局的建議考慮因素。

1. USB trace/USB 信號線

- USB differential pair traces should be routed with differential impedance of 90±15% ohms.
  USB 差動信號線的差動阻抗值應為 90±15%歐姆

- When using a common mode choke and an ESD protect part to suppress EMI and ESD, they should be placed as close as possible to the USB connector.
  使用common mode choke或ESD保護元件時，這些元件應盡量靠近USB連接器

- Never route USB differential traces near the PCB edge to prevent from the distortion of USB signal by EMI and ESD.
  勿將USB信號線擺放於PCB的板邊，以避免受到電磁干擾或靜電放電的影響

- It is recommended to straight route USB differential pair and less route them with bends as figure 1.
  一組 USB 信號線需優先佈線，並盡量以直線方式來佈線，盡量避免以轉彎的方式來佈線，如圖一所示

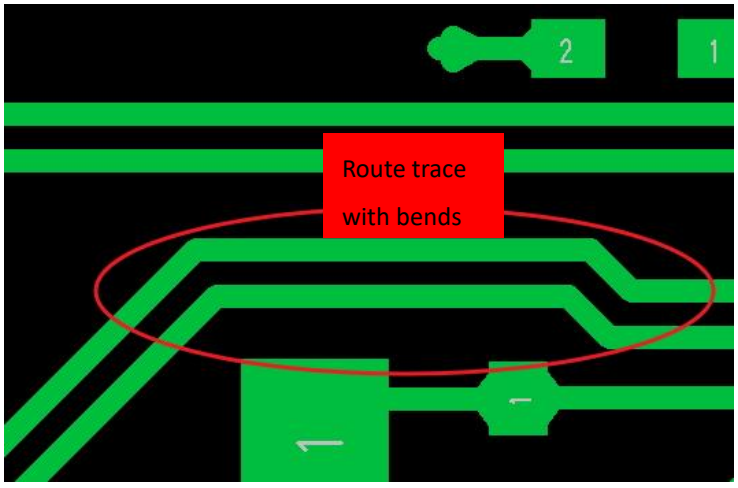

Figure 1

Besides, to avoid right angle signal traces as figure 2.
此外，信號線需轉彎時，避免採用直角(90度)方式進行佈線，改用約45度轉彎的方式來佈線，如圖二所示

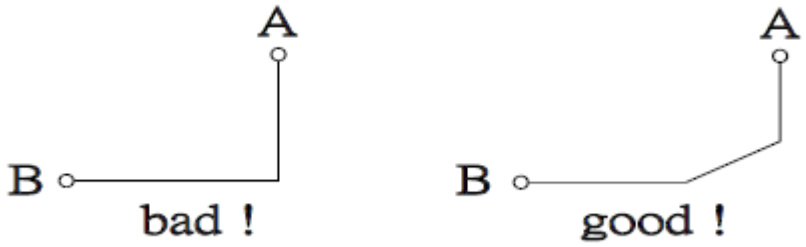

Figure 2

- Never route USB differential traces near other high frequency and power traces to avoid crosstalk between two different traces.
  勿將USB信號線靠近高頻信號線或電源迴路線，以避免被高頻信號干擾或去干擾了電源迴路線

Ways to Avoid Crosstalk/避免兩種信號間或信號與電源間互相干擾:之方法:

-Use the 3W rule (3 times the width of signal or power trace as figure 3) to separate two different traces.
將兩條走線之間距，保持三倍線寬的距離，如圖三所示

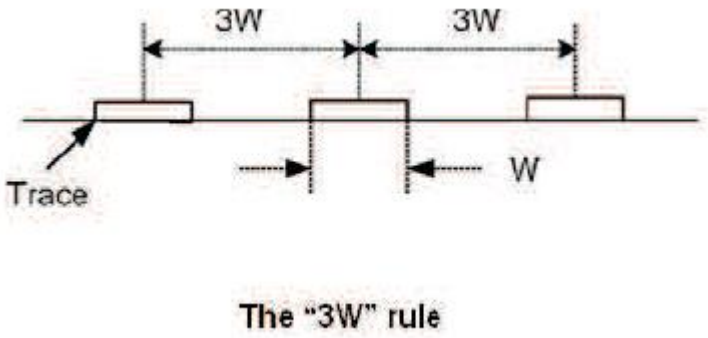

Figure 3

-Use ground traces around either USB signal or other high frequency signal traces to separate two different traces.
將干擾源與怕干擾端之間以GND走線隔開

2. Power/電源

- Place decoupling capacitors near the power pin of PL2303Gx IC.
  PL2303G 系列 IC 電源腳的解耦合(濾波電容)，需擺放在電源腳附近

- Minimum trace width of VBUS power pin of USB connector and other 5V power pins is 20 mils.
  USB連接頭的VBUS電源腳接線與其他5V電源接線的最小線寬為20 mils

- Minimum trace width of 3.3V and IO/signal power(VDD_IO) is 8 mils.
  3.3V及信號電源((VDD_IO)之電源接線的最小線寬為8 mils

- It is recommended to partition a 3.3V power plane to connect all of 3.3V power nets if there are many 3.3V power nets in your schematics.
  若電路圖中的3.3V電源接點較多，建議切割一塊3.3V power plane來連接所有3.3V接點

3. Others/其他

- The trace between crystal pins of PL2303Gx IC and the external crystal is as short as possible.
  PL2303G 系列 IC 與外部震盪器相連之接線盡量縮短

- NC pins of 4-pin crystal should be connected to GND to prevent from EMI.
  有四個腳位的震盪器之兩根 NC 腳，應接 GND，以避免成為電磁干擾源或受到電磁干擾

- Allocate the unused area of PCB as a GND plane to enlarge GND plane and keep GND plane continuous on whole PCB.
  將 PCB 的未使用區域設置為 GND plane，為了讓整個 PCB 之 GND plane 可以加大及確保不同區域 GND 可以相連(增加 GND plane 的分佈及連續性)

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