



# Engineering Change Notice

NUMBER	REV.	SHT
ECN-05042005-01A	1.0A	1 of 1

SUBJECT  Silicon Revision Change Notice (Chip Rev 1D)	PRODUCT NUMBER/NAME PL-3507 Hi-Speed USB & IEEE 1394 Combo to IDE Bridge Controller
	ECN RELEASE DATE 5/04/2005

## Contents of Notice

### Scope and Purpose

This notice is to summarize the silicon revision change for PL-3507 chip version 1D.

### Revision Change

#### ➤ Rev 1D: (Hardware Changes)

- Pin-to-pin compatible with PL-3507C. No need to change PCB if Pin 6 (GP1[7]) is connected to flash address bit 15. Also, Pin 80 (P16K) must be tied to ground if program code exceeds 16KB.
- Passed [FireWIRE and i.LINK 1394 Compliance Logo Test](#) (TA ID #200404004).
- Pin Assignment Changes – Most of NC pins (pins 81 to 86) of the PL-3507C are converted to six extra GPIO pins. Only pins 78 & 80 functions have been changed but their settings in PL-3507C won't affect the functionality of PL-3507D. Refer to the PL-3507D datasheet for more information.

Pin Number	PL-3507C	PL-3507D	Description
78	IDE_BLKEN	SCAN_IN[0]	PDMA module has been removed in PL-3507D, so "IDE_BLKEN" is no longer needed. This pin is now used for scan test input in USB PHY scan test mode.
80	FCPU_50M	P16K	This pin was used to select CPU clock when 1394 is active in PL-3507C. This pin was changed to select shadow SRAM size in PL-3507D.
81	NC	EGPIO[0]	Extra GPIO pin with positive/negative polarity trigger interrupt functionality. Set as input pin when power on. <sup>(1)</sup>
82~85	NC	EGPIO[4:1]	Extra GPIO pin with negative polarity trigger interrupt functionality. Set as input pin when power on.
86	NC	EGPIO[5]	Extra GPIO pin with negative polarity trigger interrupt functionality. Set as input pin when power on but this pin is dedicated to USB remote wake-up function.
87	NC	PGM_TEST	In PL-3507D, this pin is used to select program memory test mode – internally pulled down.

Note (1): Only EGPIO[0] can be set as positive polarity trigger interrupt pin. EGPIO[5:1] can only be set as negative polarity trigger interrupt pins.

- Auto-detection of external flash & internal ROM<sup>(2)</sup>. Program code will be loaded into the internal shadow SRAM for program execution when external program flash exists. Otherwise, the internal program ROM will be used for program execution.

Note (2): For PL-3507 Chip Rev 1D, it is still required to run from an external flash ROM.

- Improved & Enhanced Functions:
  - Retry function: PL-3507D will retry the requests if the host didn't respond the requests from the PL-3507D due to any unpredictable errors.
  - Internal ROMs.
  - Six more GPIO pins with interrupt function.
  - Hardware support for 2 logic units of 1394 for Master/Slave IDE devices (firmware not implemented and verified yet).